Anode amplifier-discriminator AD96/A (prototype).

This module is designed for anode signals of CSC and optimized for big detector capacitance (up to 300pF)
The module has 96 identical channels. Each channel consists of preamplifier, amplifier-shaper, constant fraction discriminator with adjustable threshold, controllable output pulse delay and output pulse width shaper.

1. Specification

Supply voltage		5.5V
Supply current		0.5A
Inputs :	-input spare potential	0.7V
	-static electricity protected	
	-maximum safe input DC current	1mA
	-minimum detectable signal	40fC
	-maximum detectable signal	1000fC
	-maximum allowed input signal	500pC

Transfer characteristics:

Amplifier gain	10mv/pC
Input noise	1fQ(@Cin=0pF) + Cin*0.01fC/pF
Min threshold on bench	10fC
Min. threshold on chamber	40fC

Threshold controllable with JTAG interface for each chip individually in range 0 - 2000 mV.

0mV	-maximum threshold,
1600mV	- minimum threshold
threshold control scale	- 8mv/div. (0.8fC/div)

Outputs: bipolar currents (1mA) compatible to LVDS standard
Pulse width 50 - 100ns (adjustable with screwdriver)
Pulse delay controllable with JTAG interface
min. 80ns
max. 100ns
slewing time on chamber under test pulse 4ns(max)

2.JTAG interface.

There are four SN74BCT8244 chips for JTAG control buffer.
There is the table for thresholds and delay assignment:

Bit#	17	16	15	14	13	12	11	10	9	8	7	8	5	4	3	2	1	0
Name	1OE	2OE	1A1	1A2	1A3	1A4	2A1	2A2	2A3	2A4	1Y1	1Y2	1Y3	1Y4	2Y1	2Y2	2Y3	2Y4
DD1	0	0	0	0	0	0	0	0	0	0	T31	T21	T11	T32	T22	T12	T33	T23
DD3	0	0	0	0	0	0	0	0	0	0	T13	T34	T24	T14	T35	T25	T15	T36
DD4	0	0	0	0	0	0	0	0	0	0	T26	T16	D7	D6	D5	D4	D3	D2
DD5	0	0	0	0	0	0	0	0	0	0	D1	D0	0	0	A0	A1	A2	WR

Note: it is very useful to put zeros to unassigned cells.
Special program is written to write data into JTAG control buffer.
Also there are switches to download JTAG control buffer manually.