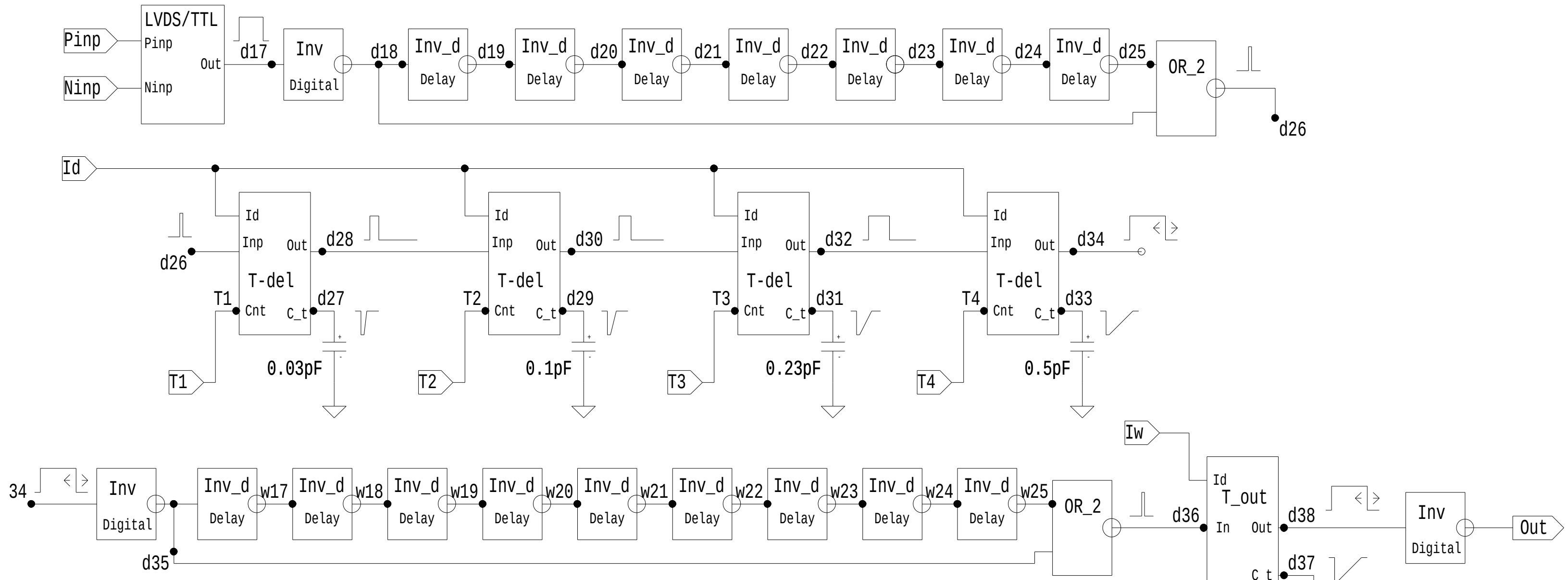
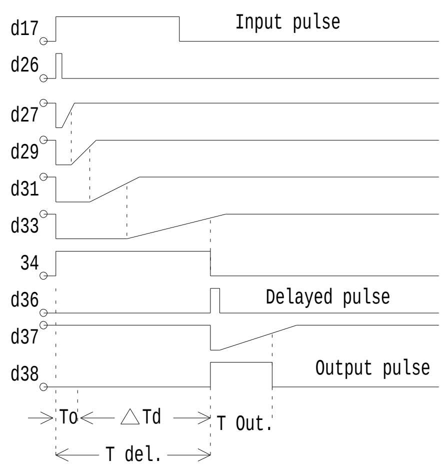


Time diagram:



Delay for each stage :

$\triangle Ti = Ci^* \triangle U/Id, \quad i=1,2,3,4$

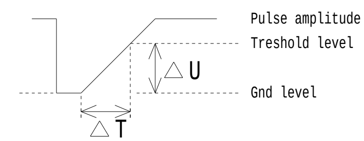
Delay for chip:

$\triangle Td = \triangle T1 + \triangle T2 + \triangle T3 + \triangle T4$

Output pulse width:

$\triangle Tout = Cout * \triangle U/Iw$

$\triangle$U - Trigger Smith threshold
$\triangle$Ti - delay time for each stage
Ci - delay capacitors
Cout - Output pulse shaping capacitor
Id - delay circuit charging current
Iw - output pulse shaping capacitor



AD16: DELAY CHANNEL	
Created:Jul 28, 1997 11:25:09 Modified:Feb 1, 2000 16:18:32	
Info:	rev. 0
Author:N.Bondar	
F:\Users\Bondar\chip2000\DEL16\DEL16 Module:DEL_CHAN	Page:Page0