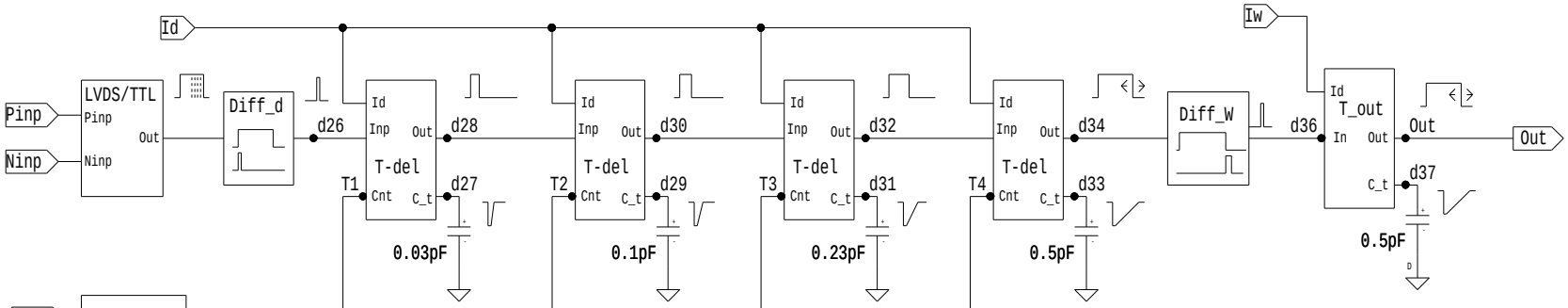
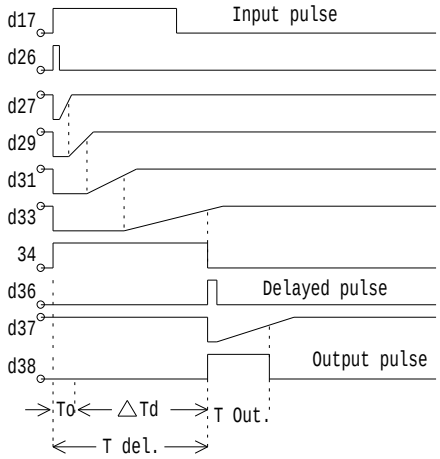
Delay chip. One channel structure.



Time diagram:



Delay for chip:

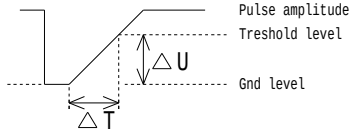
Tdel= To+ △Td

To - minimal delay of the delay circuit

△Td= △T1+ △T2 + △T3+ △T4

Delay for each stage :

△Ti = Ci* △U/Id, i=1,2,3,4



Output pulse width:

△Tout = Cout * △U/Iw

△U - Trigger Smith threshold

△Ti - delay time for each stage

Ci - delay capacitors

Cout - Output pulse shaping capacitor

Id - delay circuit charging current

Iw - output pulse shaping capacitor

AD16: DELAY CHANNEL

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Modified:Feb 14, 2000 10:06:33

Info: rev. 0

Author:N.Bondar

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