# CMS Muon Endcap CSC Anode Front-End Electronics

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# 1 Introduction.

## 1.1 Purposes.

The front-end anode electronics for the CMS Endcap Muon System has three main purposes:

- to acquire precise muon timing information for bunch crossing number identification at the Level 1 trigger and for offline analysis;
- to help in the muon trigger by requiring the muon track to point back to the interaction region;
- to provide a coarse radial position of the muon track for the offline analysis.

## 1.2 General requirements.

The general system requirements of the anode front-end readout are:

1) to perform with minimum dead-time;
2) to be able to function with a high anode wire group singles rate;
3) to function in the magnetic field up to 2 T;
4) to be reliable, compact and suitable for chamber mounting;
5) to be inexpensive on a per channel basis;
6) to generate as little heat as possible (power consumption per channel less than 200 mW);
7) to be able to withstand the radiation level in the endcap muon region (up to 1.78 krad of total ionizing dose and up to 0.62 x $10^{12}$ n/cm$^2$ of neutron fluence during the 10-year period of LHC operation with a peak luminosity of $10^{34}$ cm$^{-2}$s$^{-1}$).

Requirements 4) - 6) are related and are a consequence of the large anode channel count (a total 189,000 anode channels, including the fourth station) in the endcap muon system. Together with requirement 7), this means that the electronics must make extensive use of inexpensive and highly reliable ASICs (application specific integrated circuits) with reasonable radiation hardness.

## 1.3 Specific requirements.

There are several cruicial specific demands for the anode front-end electronics. The time between beam crossings at the LHC will be 25 ns. The CMS EMU baseline calls for the anode system to have an efficiency of at least 92% per 6-layer chamber for getting the correct beam crossing number for the muon. Therefore, the emphasis in the anode readout design was on the accuracy of timing, not in the accuracy of the pulse height as in the cathode front-end case. In particular, the shaping time of the electronics should be about 30 ns, and the time resolution, including slewing, should be less than 3 ns. In addition, the preamplifier should have low noise (7000 e$^-$'s equivalent, or about 1 fC) and a low oscillation-free threshold of 10 - 20 fC. All these parameters above (except the noise) should not depend on the relatively large input capacitance of the anode wire groups, which ranges from 20 to 150 pF over the different size chambers.

# 2 The anode front-end structure.

The anode electronics structure is presented in Fig.1 (for one channel) and includes the protection board (PB), the AD16 anode front-end board (AFEB) with its 16-channel ASIC chip CMP16F on it, the cable from the AFEB to the ALCT (Anode Local Charged Track) trigger board and, functionally related to the AFEB, parts of the ALCT board itself.

The protection boards are part of the cathode strip chambers (CSC). They are assembled on the anode side of the CSC during chamber production. Each of them delivers anode signals from 16 ganged groups of anode wires (5 to 16 wires) from two CSC layers (8+8) through a 34-pin standard input connector of the AFEB to the preamplifiers of the CMP16F chip. They also protect the CMP16F chip against high voltage sparks, using a resistor-diode scheme. There is an additional resistor-diode protection circuit at the inputs of the preamplifiers on the AFEB card.

The anode front-end board plugs directly into the protection board. The AFEB cards amplify and discriminate the anode signals and send logic pulses when the anode signal exceeds a discriminator threshold. Each AFEB is connected to a single on-chamber ALCT board via a 20-twisted-pair shielded round cable, which transmits the 16 output AFEB signals to the delay chips on the ALCT board. Using the same cable, the ALCT board provides the AFEB card with power (protected by one fuse per each AFEB), ground, a threshold level, a test pulse (delivered to the input of all amplifier channels simultaneously) and a power standby level used to disable a CMP16F chip in case of latch-up or oscillations. Any hot or dead AFEB channels can also be masked on the ALCT board before they are read out.

# 3 Amplifier-discriminator chip CMP16F.

## 3.1 Description.

The main part of the anode front-end electronics is an amplifier-discriminator microcircuit. The structure of this circuit is presented in Fig.2 and a functional circuit diagram in Fig.3. This is a three-stage amplifier-shaper, followed by a two-threshold discriminator.

The amplifier-shaper consists of a charge-sensitive preamplifier, a tail cancellation circuit and a two-pole active filter. It produces an output signal sufficient for a stable threshold characteristic of the discriminator.

In this scheme, a high-threshold discriminator is driven by the initial signal from the amplifier. The threshold level of the discriminator is adjustable from 0 to 70% of a nominal input signal of 142 fC, with an accuracy of the first base line restorer. The resulting pulse enables the precision-time discriminator, which consists of a constant-fraction shaper and a low-level discriminator. The constant-fraction shaping is done by adding the differentiated amplifier signal and the corresponding inverted and attenuated signal. The resulting signal is further amplified and delivered to the input of a zero-crossing discriminator. The zero-crossing point corresponds to approximately half the rise time of the input signal. The threshold of the zero-crossing discriminator is set to zero with an accuracy of the second base line restorer. The LVDS compatible output signal (current of 1.5 ma) has a width in the range of 40 - 100 ns depending on the signal over threshold time. Table 1 lists the design specifications for the anode amplifier-discriminator circuit.

One chip contains 16 identical channels. Each channel has a test capacitor of $\sim 0.25$ pF connected to the input node of the channel. This capacitor is used for calibration with the test pulse.

Several versions of the amplifier-discriminator chip based on these specifications have been designed using a BiCMOS 1.2 micron technology and were prototyped in the AMI foundry through the MOSIS program.

The latest chip prototype makes use of a BiCMOS 1.5 micron technology. The chip package is an 80-pin Quad Flat Pack with a pin pitch of 0.8 mm. A full set of electrical circuit diagrams are given in Attachment 1.

# 4 Anode front-end board AD16.

## 4.1 Specifications.

The AD16 board is a 16-channel amplifier - discriminator board for the anode signals of the CSC chambers. It carries one CMP16F chip (see Fig.4). This board is designed for direct connection to the protection board of the CSC. The specifications of the board are given in Table 2.

The assembly drawing is presented in Fig.5, and a circuit diagram of the board with input and output connector specifications are given in Fig.6.

## 4.2 Specifications from on bench test.

The total of 28 AD16 boards with CMP16F chips were tested on the ASIC test stand at Fermilab. The results are shown in Table 3.

## 4.3 Chamber fixation of the AFEB, the AFEB to ALCT cable and cooling.

Each AD16 board is directly connected to a protection board on the chamber. The AD16 position on the chamber is shown in Fig.7. Despite the fact that the AD16 input connector does not have a polarization key, it is impossible to plug the fully assembled AD16 board into the protection card in the wrong way. The board sticks out of the side of chamber via a slot in the CSC side panel. A special bracket is attached to the panel next to the slot to fix the board and provide additional grounding between the board and the chamber. All AD16 boards on the chamber will be covered by an aluminium cover for additional shielding and mechanical protection.

The AFEB - ALCT cables (halogen free) are grouped into sets of different lengths to accommodate the different distances between sets of AD16 boards (3 boards per column) and the ALCT. They have strain relief on both ends. Each type of CSC has its own cable layout and individual cable sets.

The amount of power consumed by all AD16 cards on one CSC chamber does not exceed 24 W. In addition, the boards are distributed along the anode side of the chamber. Therefore, the chamber design has no water cooling for the anode front-end boards. In a test, the temperature increase of a CMP16F chip on an AD16 board plugged into a chamber did not exceed 10° C relative to the ambient air temperature.

# 5 Delay chip.

There is a significant time spread of anode signals arriving at the ALCT board caused by such things as different times-of-flight from the interaction region to the chambers, variations in processing time in the preamplifier-discriminator chips and in propagation time from the AFEB to the ALCT (different lengths of AFEB - ALCT cables). To obtain optimum bunch crossing tagging efficiency, a fine delay control is needed to change the phase of the anode signals with respect to the LHC clock. For this purpose, a custom designed 16-channel delay ASIC chip was produced. Using the ALCT control, the chip allows the delay of anode signals over a range of 32 ns, in 2 ns steps. Furthermore, the output of the AD16 chip is an LVDS signal, while the required input to the ALCT FPGA's is CMOS. So this delay chip also does the LVDS-to-CMOS level conversion.

The structure of one channel of this chip is shown in Fig.8. Each channel consists of a input LVDS-to-CMOS level converter, four stages of delay (1, 2, 4, 8 steps), an output width pulse shaper and a serial interface to the delay control. The interface structure is given in Fig.9. The chip was designed using a

0.5 micron CMOS technology and was prototyped at the AMI foundry via the MOSIS organization. The chip is packaged in a 64-pin Quad Flat pack with a pin pitch of 0.5 mm. The chip size is 10 mm x 10 mm. A full set of electrical circuit diagrams can be found in Attachment 2. The list of specifications for the delay chip as measured on the ASIC test stand is given in Table 4. All 16 channels of the chip are controlled simultaneously.

## 6 Tables

Table 1. Anode amplifier-discriminator ASIC design specifications.

| | |
|---|---|
| Amplifier input noise | 0.5 fC @Cin=0 (1.7 fC @Cin=200 pF) |
| Shaper peaking time | 30 ns |
| Shaped waveform | Semi-gaussian with two-exponent tail cancellation |
| Transfer function (gain) | 5 mV/fC |
| Two threshold discriminator | High threshold used as ENABLE. Low threshold zero-crossing discriminator driven by a constant-fraction shaped pulse. |
| High level threshold | Adjustable, 0 - 500 mV |
| Discriminator slewing time | 3 ns |

Table 2. Anode front-end board AD16 specifications.

| | |
|---|---|
| Board dimensions | 2.8" x 3.075" x 0.625" |
| Input connector | strip socket, two rows, 34 contacts |
| Output connector | 40-pin header with polarized key |
| Inputs | DC isolated |
| Outputs | current source LVDS compatible |
| Input power supply voltage | +5.5 V<br>+4.0 V minimum<br>+6.0 V maximum |
| Current | 0.09 A @+5.5 V |
| Power consumption | 495 mW total<br>31 mW per channel |
| Input threshold voltage | from 0 to 1.7 V control range<br>0 corresponds to maximum threshold |
| Input test pulse: | negative, from 0 to $-2$ V<br>110 Ohm termination<br>0.25 fC/mV transfer function<br>20 ns rise time<br>$> 2$ $\mu$s pulse width |

Table 3. Measured specifications of the amplifier-discriminator ASIC.

| | |
|---|---|
| Amplifier input noise | 0.7 fC @Cin=0 (1.5 fC @Cin=180 pF) |
| Transfer function (gain) | 9 mV/fC |
| Minimum stable threshold | 5 fC (on the bench) |
| Threshold temperature variation | -0.5 fC/degree C (preliminary) |
| Discriminator slewing time | 2.3 ns at $Q_{thr}$ = 17 fC and $Q_{in}$ = 50 - 600 fC |
| Output pulse width | 60 ns (average) |

Table 4. Delay chip specifications

| | |
|---|---|
| Input signal level | LVDS standard |
| Output signal | 3.3 V CMOS |
| Delay minimum | 20 ns |
| Delay step $\Delta$T | 2 ns (adjustable with an external current) |
| Delay step number N | 15 maximum |
| Delay function | 20 ns+N$\star\Delta$T |
| Delay nonlinearity | $\pm$ $\Delta$T/2 |
| Output pulse width | 40 ns (adjustable with an external current) |
| Power supply voltage | + 3.3 V |
| Control interface signal specifications: | |
| CLRB | Set delay to zero |
| ChSB | Select chip to download delay data. Data is fixed inside the chip at the end of the ChSB pulse. |
| CLC | Clock pulses |
| D_IN | Input data pattern |
| D_OUT | Output data pattern |