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NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

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Anode front-end electronics for the cathode strip chambers of the CMS Endcap Muon detector

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Abstract

The front-end electronics system for the anode signals of the CMS Endcap Muon cathode strip chambers has about 183,000 channels. The purposes of the anode front-end electronics are to acquire precise muon timing information for bunch crossing number identification at the Level-1 muon trigger system and to provide a coarse radial position of the muon track. Each anode channel consists of an input protection network, amplifier, shaper, constant-fraction discriminator, and a programmable delay. The essential parts of the electronics include a 16-channel amplifier–-shaper–discriminator ASIC CMP16 and a 16-channel ASIC D16G providing programmable time delay. The ASIC CMP16 was optimized for the large cathode chamber size (up to $3 \times 2.5\,\mathrm{m}^2$) and for the large input capacitance (up to 200 pF). The ASIC combines low power consumption (30 mW/channel) with good time resolution (2–3 ns). The delay ASIC D16G makes possible the alignment of signals with an accuracy of 2.2 ns. This paper presents the anode front-end electronics structure and results of the preproduction and the mass production tests, including radiation resistance and reliability tests. The special set of test equipment, techniques, and corresponding software developed and used in the test procedures are also described.
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Keywords: CMS; Endcap muon cathode strip chambers; Anode front-end electronics structure and mass production test

1. Introduction

The Compact Muon Solenoid (CMS) experiment [1] at CERN is designed to trigger on and reconstruct muon tracks at the highest luminosities of the Large Hadron Collider (LHC). The

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cathode-strip chambers (CSCs) of the CMS Endcap Muon system [2] provide the high coordinate precision and fast response time needed for effective bunch crossing number identification. The CSCs [3] are six-layer, two-coordinate-measuring, multiwire-proportional, cathode-strip chambers separated by the iron disks of the flux return yoke of the CMS magnet. In a CSC layer, the anode wires are in the azimuthal direction and the cathode strips are in the radial direction.

The front-end electronics for the CSC has two main purposes: (1) to acquire precise muon position and timing information for offline analysis; and (2) to generate muon trigger primitives for the Level-1 trigger system. The organization of the front-end electronics is schematically shown in Fig. 1. The signals from the cathode strips are read out by the cathode front-end electronics [4] providing the precise measurement of the azimuthal coordinate of the hit for offline analysis. The trigger part of the cathode front-end boards (CFEBs) gives for each CSC the coarse time, azimuthal location, and angle of the local track, which are used as trigger primitive parameters by the Level-1 muon trigger system.

The focus of the design of the anode front-end electronics was on the accuracy of timing. The anode front-end electronics supplies precise timing measurement of an anode wire hit, as well as a coarse measurement of its radial position. The large spread of the anode drift times with a maximum of 50 ns is overcome by the requirement to have a coincidence of more than three layers for anode wire hits forming the predefined track patterns. The best definition of the LHC beam bunch crossing time of 25 ns in this case is given by the use of the time of the second or even the third or fourth earliest anode hit [2,3]. This procedure is less vulnerable to random hit backgrounds than using just the first hit and provides a high-efficiency bunch crossing identification, the formal requirement being 92% per CSC [2]. The corresponding algorithms are implemented in the anode local charged track (ALCT) board [5] located on

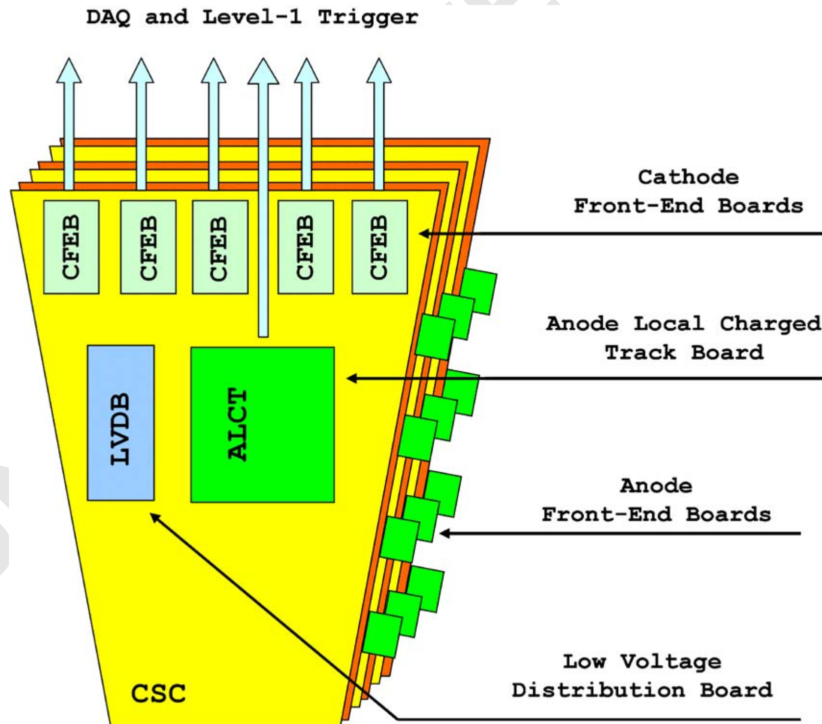

Fig. 1. Schematic view of the front-end electronics on an Endcap Muon CSC chamber.

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each CSC that receives signals from the Anode Front-End Boards (AFEBs). The ALCT identifies the radial location, bunch crossing time, and quality of the best two tracks for each CSC and passes these parameters to the Level-1 trigger system. It also sends out the raw list of CSC wire hits.

As a part of the CMS detector, the anode front-end electronics should satisfy the corresponding performance requirements and special conditions [2]. The large number of channels and the long-term operation time of the LHC (at least 10 years), with limited maintenance and repair access, require very high reliability of the anode front-end electronics. The system should be able to also withstand the radiation and interaction background levels expected in the Endcap Muon region. To provide highly efficient 25 ns bunch crossing number identification, the resolution time of the anode electronics should not exceed 2–3 ns, including the contribution from the slewing time of the electronics.

Other important considerations for the anode front-end system are ([2]) as follows:

- function with high wire singles rate (up to 20 kHz/channel);
- low power consumption (less than 200 mW per channel);
- compact and suitable for chamber mounting;
- inexpensive on a per channel basis.

The design of the anode front-end electronics should also take into account the special features of the CSCs, such as their large size (up to $3.4 \times 1.5\,m^2$) and large detector capacitance per channel (up to 200 pF) created by ganging together anode wires (5–16 wires per 1.6–5.1 cm wide wire group).

In this paper, we present the structure of the CSC anode front-end electronics (Section 2) and results of the pre-production tests, including chamber performance, radiation resistance, and reliability tests (Section 3). The mass production testing, using a special set of test equipment, techniques, and corresponding software, is described in Section 4. Some parts of this work have been previously published elsewhere [6–8].

2. Anode electronics structure

2.1. General scheme

The structure of one channel of the anode front-end electronics is shown in Fig. 2. To achieve a minimum stable threshold level with the minimum possible crosstalk, the standard structure of the anode electronics channel was split into three parts located on three different boards. In addition, the amplifier–chamber signal connection and the chamber grounding and shielding were carefully planned and executed.

The input signal from a group of CSC wires goes through the Protection Board (PB) to the 16-channel anode front-end board (AFEB). The Protection Board is a part of the chamber assembly. It is located on the signal side of the CSC and is soldered to the anode wire network.

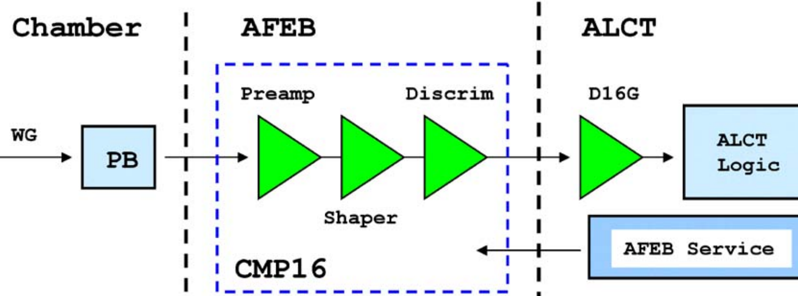

Fig. 2. Anode electronics structure. WG: anode wire group; PB: protection board; AFEB: anode front-end board; ALCT: anode local charged track board.

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The AFEB plugs directly into the PB. The main component of the AFEB is a 16-channel amplifier–shaper-discriminator ASIC (application-specific integrated circuit) CMP16[1]. The output of the AFEB is connected to the ALCT board by a twisted-pair cable. There is one ALCT board per chamber and it accepts signals from 12 to 42 AFEB boards, depending on the size of CSC. The ALCT also provides power and other service voltages to the AFEBs. At the input of the ALCT, the signal is delayed by a 16-channel programmable delay ASIC, D16G. Placing the digital ASIC on the ALCT board rather than making it a part of the amplifier ASIC minimizes the crosstalk to the input analog part of the CMP16 and reduces the CMP16's power consumption. Standard 1.5 μm BiCMOS (Bipolar CMOS) and 0.5 μm CMOS (complementary metal oxide semiconductor) technologies were used for designing the ASICs, resulting in a relatively low price with sufficient radiation hardness.

2.2. Chamber grounding and shielding

For each CSC layer, the anode wire plane is placed between two cathode planes, one with cathode strips milled into the copper-clad panel surface, while the other is free of strips and serves as a clean signal ground for both the anode and cathode electronics input circuits. Both the anode and cathode amplifier input ground terminals are connected to this plane. The two outermost copper-clad panel surfaces, together with the aluminum side frame and side covers, constitute the radio-frequency (RF) case shielding for the entire chamber. The RF case and the signal ground of each plane are interconnected at the amplifier side of the chamber to form one L-shaped continuous line of interconnection to avoid a ground loop through the signal ground and along the amplifier input ground circuit [2].

The chamber anode wires, cathode planes, protection boards, and even the cathode amplifier input connections affect the anode front-end electronics performance, all being effectively parts of the anode amplifier input circuit. To obtain optimal performance of the chamber, the following rules were observed:

- the anode amplifier input impedance must be close to the anode wire structure characteristic impedance;
- the cathode amplifier input impedance must be close to the characteristic impedance of the cathode strip structure;
- the detector–amplifier ground connection should be as short as possible and as wide as possible to have the minimum possible impedance for the connection [9].

2.3. Protection board

The specially designed protection board (PB) [10] has two functions. The first is to fan-in the chamber anode signals and adapt them to the standard 34-pin connector for the AFEB. The PB is mounted on the chamber panel edge, takes signals from 8 + 8 wire groups in two neighboring anode planes, and brings them to a 34-pin connector where the 16-channel AFEB is plugged in. The PB also provides a proper ground connection between the chamber signal ground and the amplifier input ground.

The second function of the PB is to protect the input of the amplifier should a spark occur in the chamber. The corresponding resistor–diode protection stage placed on the PB minimizes the spark current loop. There is one more such stage on the input of the AFEB providing additional protection (Fig. 3). A preproduction prototype of the PB was successfully tested and showed no failure after 100,000 sparks produced from discharges at 5 kV of a 1 nF capacitor through a 25 Ω resistor.

2.4. Anode front-end board

The 16-channel AFEB AD16 [11] was designed to hold the CMP16 ASIC (Fig. 4). The board receives the signals from the anode wire groups, amplifies them, and selects the signals that are over the preset threshold with precise time accuracy.

[1] CMP16 is an abbreviation for the 16-channel ASIC designed by a collaboration of Carnegie Mellon University and Petersburg Nuclear Physics Institute.

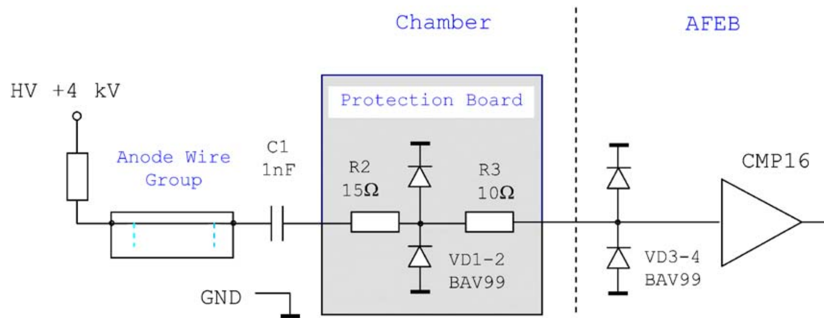

Fig. 3. Schematic diagram of the protection circuit.

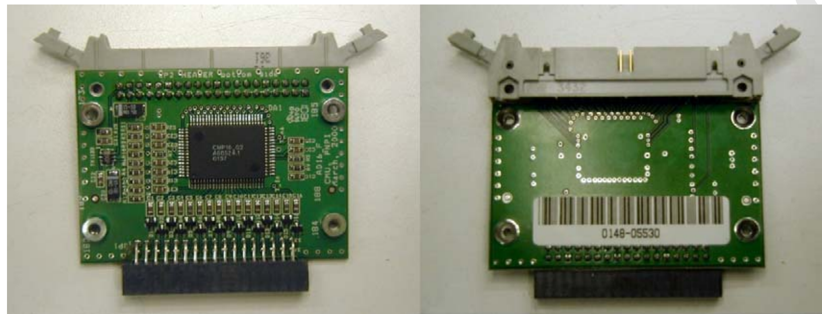

Fig. 4. (a) Top view of AFEB AD16. (b) Bottom view.

The output logic signals with standard low-voltage differential signaling (LVDS) levels are transmitted to the ALCT. The simple and cost-effective design of the AFEB matched the scale of the mass production and testing of more than 12,000 boards. The board has two layers (one of which is ground) and on it are one CMP16 chip and a minimum number of service components, including a small voltage regulator TK112B (TOKO America, Inc., Mt. Prospect, IL, USA) with current overflow and overheating protection and a "power-on/off" feature. The AFEB also has a special test input that is connected to the internal capacitance of each channel of the CMP16 ASIC. The amplitude-controlled test pulse from the ALCT's test pulse generator fires simultaneously all 16 channels of the CMP16, and allows the monitoring of the thresholds and functionality of the AFEB.

A 34-pin input connector and a 40-pin output connector are located on opposite sides of the board to minimize output-to-input crosstalk. The size of the board is $71 \times 79\,\text{mm}^2$. The board also has an aluminum cover with a thermo-conductive pad between the ASIC and the cover (not shown in Fig. 4). The cover protects the board and provides heat dissipation. The power consumption of the board does not exceed 0.6 W at a voltage of 5.0 V. The board is plugged into the PB and is fixed on the chamber assembly side cover with a special bracket providing a reliable junction (Fig. 5). There is an additional chamber side cover protecting all the AFEBs and adding more shielding (not shown in Fig. 5).

A halogen-free shield-grounded 20-pair twisted-pair cable (Amphenol Corporation, Wallingford, CT, USA) connects the AFEB with the ALCT board. This cable is used to both transmit output signals to the ALCT and supply the AFEB with power voltage, discriminator threshold voltage, and the test pulse. The ALCT provides the following AFEB services [5]: a power supply voltage distribution circuit, a "power-on/off" command driver for each AFEB, and a threshold

control voltage source for each AFEB that applies a threshold voltage to all 16 channels on the board. There are six other test outputs on the ALCT, each one connected to a special test cathode strip located at the edge of each cathode plane. A test pulse is injected onto the test cathode strip, which induces an input charge on all the perpendicular anode wire groups of a given CSC layer. Such a scheme provides a test of each anode channel's connectivity and plane-to-plane cross-talk.

2.5. Amplifier ASIC CMP16

The ASIC parameters were specially optimized for the CSC in order to obtain optimal performance. To achieve accordance between a large detector size and a large detector capacitance on the one hand and high sensitivity and time accuracy on the other hand, a relatively long shaping time of 30 ns for the anode signals, together with a two-threshold constant-fraction discriminator, was proposed and used. This shaping time gives an amplifier input charge of about 12% of the total charge collected by the anode wire [12]. For a discriminator threshold as low as 20 fC, the efficiency plateau starts at 3.4 kV for a gas mixture of Ar(40%) + CO_2(50%) + CF_4(10%) [3]. The nominal high-voltage operating point of the chamber is typically 3.6 kV.

Fig. 5. A view of the anode front-end boards installed on a chamber. Also shown are the AFEB–ALCT cables.

The circuit block diagram of one CMP16 amplifier–shaper–discriminator channel is presented in Fig. 6. In this scheme, an output of the high-level discriminator serves as the enable pulse for the precision time discriminator. The precision time discriminator consists of a constant-fraction shaper and a low-level discriminator. The constant-fraction shaping is done by adding the differentiated amplifier signal and the corresponding delayed and inverted signal. The resulting pulse is further amplified and delivered to the input of a low-level discriminator. The threshold of the low-level discriminator is used for adjusting the start time of the output pulse and minimizing the slewing time. One chip contains 16 identical signal channels and one special test channel. Each

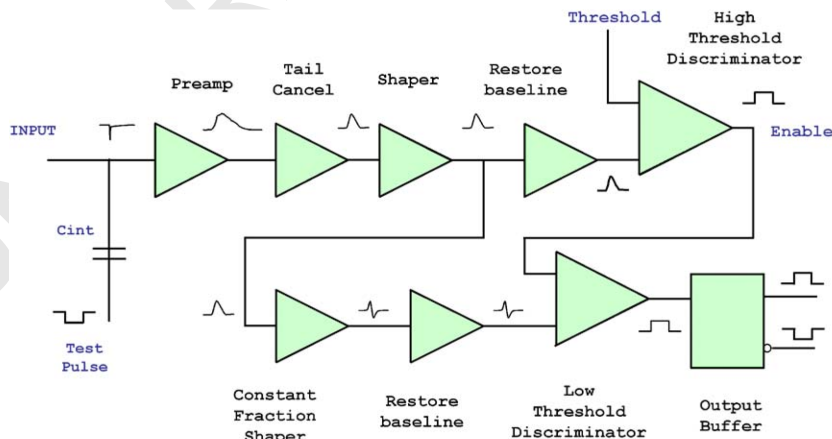

Fig. 6. Circuit block diagram of one CMP16 amplifier–shaper–discriminator channel (schematic diagram is available in Ref. [13]).

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signal channel has a test capacitor (C_{int}~0.24 pF) connected to the input node of the amplifier.

The basic characteristics of the ASIC are presented in Table 1. The values of the dynamic parameters are defined as the mean of the corresponding distribution for all AFEBs boards that passed the mass production test (see Section 4).

The CMP16 was designed using a BiCMOS 1.5 μm technology and was made at the AMI foundry (American Microsystems, Inc., Pocatello, ID, USA) through the MOSIS Service (University of Southern California Information Sciences Institute, Marina del Rey, CA, USA). The chip package is a plastic 80-pin Quad Flat Pack with a pin pitch of 0.8 mm. The chip size is $14 \times 20\,mm^2$.

Table 1
CMP16 characteristics

Input impedance	40 Ω
Transfer function (gain)	6.9 mV/fC
Amplifier input noise	0.7 fC at $C_{det} = 0$ pF, 1.4 fC at $C_{det} = 180$ pF
Shaper	30 ns peaking time, semi-Gaussian with 2-exponent tail cancellation
Discriminator	2threshold zero-crossing constant-fraction discriminator
Propagation time	67 ns at 100 fC input charge
Slewing time	3.0 ns for 60–600 fC input charge and 30 fC threshold
Resolution time, RMS	0.6 ns at 100 fC input charge and 30 fC threshold
Threshold control	0–1.2 V (7–180 fC input charge)
LVDS output pulse width	Input pulse width over the threshold, 25 ns minimum
Voltage, power	4.7–5.2 V (5 V on AFEB), 0.5 W/chip

2.6. Delay ASIC D16G

The anode signals arriving at the ALCT have a significant variation of phase due to variation in cable length, muon flight time, and propagation time of the CMP16. The maximum time variation can be up to 20 ns in large chambers. To align the input pulse phases, a special 16-channel control delay chip was designed as an input circuit of the ALCT (Fig. 7).

Each channel consists of an input LVDS-to-CMOS level converter; four capacitor-based stages with delays of 1, 2, 4, and 8 steps; and an output width pulse shaper. Moreover, the chip can generate a test level at each output. This option is used to test the ALCT. The chip has a serial interface to control the delay and set the output test level. The parameters of the D16G chip are given in Table 2. The values of the dynamic parameters are defined as the mean of the corresponding distribution for all chips that passed the mass production test (see Section 4).

The chip was designed using AMI CMOS 0.5 μm technology and was made in the AMI

Table 2
D16G characteristics

Input	110 Ω, LVDS
Output signal	3.3 V CMOS, 40 ns pulse width (adjustable)
Delay for code 0	22 ns
Delay step	(1.5–3) ns/LSB (adjustable)
Delay control	4 bits (15 steps)
Temperature drift	0.6 ns/10 °C
Voltage, power	3.3 V, 0.2 W/chip

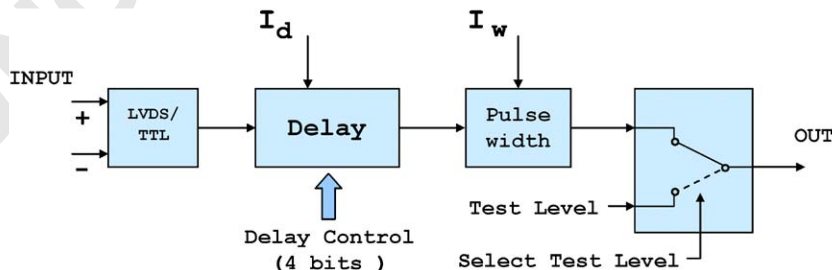

Fig. 7. Circuit block diagram for one channel of the D16G (schematic diagram is available in [14]). I_d and I_w are the currents used to control the delay step and the output signal width.

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foundry via the MOSIS Service. The chip is packaged in a plastic 64-pin Quad Flat Pack with a pin pitch of 0.5 mm. The chip size is $10 \times 10\,mm^2$.

3. Anode electronics preproduction tests

3.1. On chamber performance

The performance of the anode front-end electronics has been successfully tested on the largest size CSC chambers using a cosmic muon test stand at Fermilab and a muon test beam at CERN. The anode wire single-layer efficiency of a CSC versus high voltage at 2 preamp thresholds of 20 fC and 40 fC is shown in Fig. 8. At a threshold of 20 fC and with a gas mixture of Ar(40%) + CO_2(50%) + CF_4(10%), the efficiency plateau starts at 3.40–3.45 kV. Increasing the threshold by 20 fC shifts the plateau up by about 130 V.

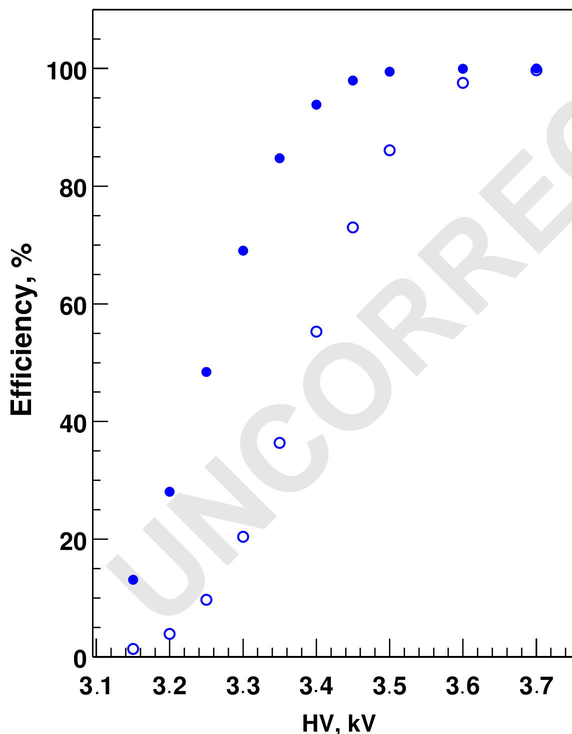

Fig. 8. CSC single-plane anode efficiency vs. high voltage with a threshold of 20 fC (filled circles) and 40 fC (open circles).

As was mentioned earlier, the time distribution of anode signals from a single chamber layer is too wide (RMS∼11 ns) to provide effective 25 ns bunch crossing identification. Using the time of the second, third, or fourth earliest hit out of six chamber hits forming a track-like pattern makes the time distribution much narrower (RMS∼5 ns) [3]. As a result, the bunch crossing tagging efficiency rises well above the baseline 92% level practically at the beginning of the plateau at 3.4 kV (Fig. 9).

A full-scale prototype CSC, completely equipped with front-end electronics, was tested in a 200 GeV muon test beam at the Gamma Irradiation Facility (GIF) at CERN. The GIF allows one to overlay muon tracks with a high rate background of 0.66 MeV photons emitted by a 0.7×10^{12} Bq Cs^{137} source. The results are presented in Fig. 10. The bunch tagging efficiency remains sufficiently high as the rate of random hits approaches and exceeds the LHC expected level (∼20 kHz per channel).

The results from the chamber tests also confirmed that the timing provided by the anode

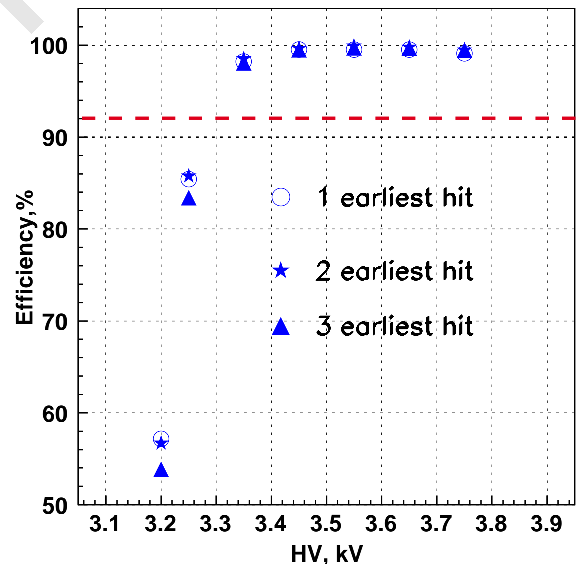

Fig. 9. Anode wire trigger performance vs. high voltage on a chamber: the probability of tagging the correct bunch crossing by using the first, second, and third earliest hits in the local charge trigger pattern [3]. The 92% baseline is shown by the dotted line.

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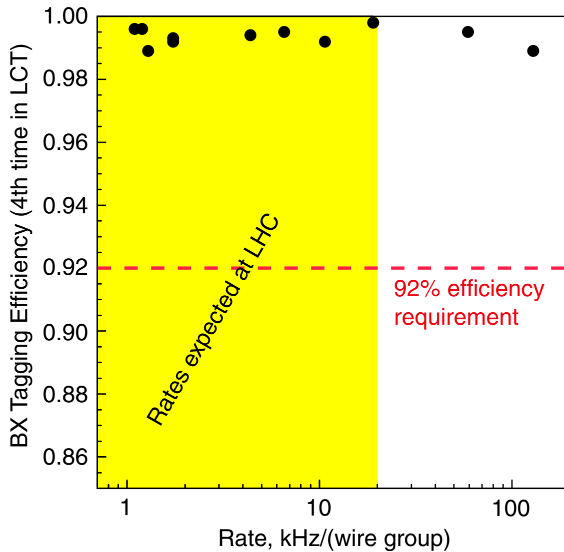

Fig. 10. Anode wire readout trigger performance (probability of tagging the correct bunch crossing by using the fourth earliest hit in the local charge trigger pattern) vs. random hit rate. The expected LHC rate is shown by the shaded area and the benchmark efficiency is shown as a dotted line [3].

front-end boards is within the design specifications.

3.2. Crosstalk

A detailed study of crosstalk was performed on the AFEB test stand and on the CSC cosmic muon test stand. The crosstalk from the signal channels to the analog test channel of the AFEB was measured, making it possible to distinguish the separate contributions of the analog and digital crosstalk. To separate the analog part of the crosstalk, the thresholds of all 16 signal channels were set to the maximum value. The amplitude of the crosstalk signal on the AFEB test channel was then measured with an oscilloscope. The input charge was varied up to 100 fC per channel. The source of the analog portion of the crosstalk is the input signal and the corresponding coefficient for the channel-to-channel isolation of the AFEB input network was found to be ~0.5% in the measurements on the AFEB stand and on the chamber. The digital crosstalk is caused by feedback from the digital output of the discriminator to the inputs of the AFEB. Given the design of the AFEB and the fixed amplitude of the discriminator output signal, the crosstalk is sensitive to the quality of the AFEB–ALCT connection and the quality of the AFEB and ALCT grounding. The contribution from one fired discriminator to the crosstalk on the test channel was found to be ~1 fC.

The AFEB's signal-channel-to-signal-channel crosstalk was directly measured on the AFEB test stand by firing one by one the signal inputs of all 16 channels of a board. The equivalent input charge of the test pulse was varied up to a large value of Q_{in} ~100,000 fC. The thresholds of all channels were set to Q_{thr} ~20 fC. The crosstalk for a given channel was then defined as the ratio Q_{thr}/Q_{in} for the value of Q_{in} corresponding to 50% efficiency for that channel to fire. The observed maximum crosstalk coefficient was ~0.8% for channels adjacent to the fired one and ~0.2% for channels next to the adjacent ones.

The probability for a channel to fire due to crosstalk at a given threshold and noise level depends on the crosstalk coefficients and the size of the crosstalk source signal. Since one AFEB serves 8 + 8 channels of two adjacent anode planes, there is a probability to observe a plane-to-plane crosstalk. To estimate such crosstalk, data with cosmic muons were taken on a fully equipped large CSC chamber having a high voltage of 3.8 kV only on the even planes and the anode thresholds set at ~20 fC. The average crosstalk was measured as the fraction of events having at least one hit in the corresponding adjacent anode plane with HV = 0. It was found to be less than 1%. At the nominal working high voltage of 3.6 kV, the plane-to-plane average crosstalk is expected to be significantly less.

The measurement of the plane-to-plane anode crosstalk is part of the chamber performance mass testing procedure at all the CSC assembly test sites [15]. For this test the ALCT generated test pulses are applied to the cathode test strip of each CSC layer in turn to check connectivity in the corresponding anode plane and observe any crosstalk in the adjacent plane. The equivalent charge induced on each of the 8 channels is about 60 fC for the largest CSC chambers. Typically, the observed

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crosstalk probability per anode channel in an adjacent plane was significantly less than the allowed upper limit of 5%.

3.3. Reliability test

To measure the reliability of the AFEB, we put 100 AFEB boards (1600 channels) into an oven at a temperature of 110 °C. The boards were supplied with power and the thresholds on the boards were set to minimum to start self-oscillations. Total test time in the oven was 4000 h (about 24 weeks). This time corresponds to about 7.5 years of real operation at 30 °C assuming that for each 20 °C the failure rate increases by about a factor of 2 [16]. Every 2 weeks the boards were taken out of the oven and the board parameters were measured on the test stand at room temperature. During the test, we have no failures and there were no visible changes in the parameters of the boards.

3.4. Radiation tolerance test

Radiation tolerance and reliability are important issues for the CMS electronics, including the Endcap Muon CSC anode front-end electronics. The peak luminosity of LHC, $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, combined with the 7 TeV beam energy, will create a very hostile radiation environment in the detector experimental hall. The most severe conditions in the CMS muon Endcap region are near the ME1/1 CSC chambers. Here, the neutron fluence and the total ionizing dose (TID) accumulated during 10 years of LHC operation (5×10^{7} s) are expected to be about $6\text{–}7\times10^{11}\,\mathrm{n/cm^2}$ (at neutron energies $E_{\mathrm{n}}>100$ keV) and 1.8–2 krad, respectively [17,18]. For CSC locations other than the ME1/1 chambers, behind the iron disks, the doses are at least 10 times lower. All but the ME1/1 CSC chambers are equipped with the AFEB AD16. However, the anode front-end boards of ME1/1 chambers also have the CMP16 chips installed on them.

With BiCMOS and bipolar components, the AFEB's ASIC chip and voltage regulator TK112B are affected by exposure to both ionizing radiation and to neutrons (displacement damage for bipolar devices), yielding degraded performance and even failure if the doses are sufficiently high. The corresponding effects are cumulative. The other major category is single-event effects (SEEs), which are caused by nuclear reactions of charged hadrons and neutrons in the devices. From these, the relevant effect is single event latch-up (SEL), which results in a destructively large current draw.

According to the plan for radiation tests of the CMS Endcap Muon electronics [19], the performance of samples of the preproduction anode front-end boards were tested up to a radiation level 3 times more than the doses expected for the ME1/1 chambers. Tests at higher doses were also done to measure the single-event latch-up rate. The boards were irradiated with a 63 MeV proton beam at the University of California, Davis cyclotron to test them for TID and SEL effects. The doses were up to 80 krad and the beam covered all elements of the board. The description of the 63 MeV proton beam test facility can be found in [20]. The purpose of the test with neutrons from a reactor at the Ohio State University was to expose the boards to possible displacement damage. The preproduction ASIC CMP16F chips were installed on the boards.[2] The details of each test are given below.

3.4.1. Tests with 63 Mev protons

Four powered anode front-end boards were tested in a 63 MeV proton beam. Two boards received seven successive exposures for approximately 1 min each, for a total TID of 14 krad. Two other boards received correspondingly seven (10) successive exposures for a total TID of 80 krad (74 krad) at approximately 1–2 min per exposure. The static parameters (voltages on the amplifier and discriminator of the ASIC and on the regulator TK112B) were measured during each exposure. The measurements of the threshold, noise, gain, discriminator offset, resolution time, and slewing time were done during 10–20 min after each exposure with the use of the ASIC test stand.

No latch-ups or spikes or any changes in the static parameters were observed. However, the dynamic parameters such as gain, offset, threshold, and slewing time were slightly sensitive to the

[2] Mass production ASIC chips were CMP16G.

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radiation. The observed threshold measured in terms of input charge decreased with TID due to changes in the amplifier gain and the discriminator offset. The overall effect on the threshold is about 15% for a TID of 60 krad. The noise increased by less than 10%. The resolution time was not affected. The slewing time showed a maximum increase of 40% at a TID of 60 krad. At the required three times level of TID (5–6 krad), all changes were practically negligible. However, at a TID of 65–70 krad, two boards failed (no output signal) showing large changes in the amplitude and the shape of the pulse after the shaper. About a month later, however, these boards had become operational again, showing that an annealing effect was present. Details of the tests are available in [7].

3.4.2. Neutron irradiation of the anode boards

In the first (preliminary) test, four unpowered boards were exposed to reactor neutron fluences of (1.2, 1.8, 3.0 and 3.6) $\times 10^{12}$ n/cm^2 at a neutron energy in the interval of 100 keV–10 MeV. The boards also received a TID of 30–150 krad from the gamma rays that accompanied the reactor neutrons. The corresponding times of the exposures were 4–24 min. The characteristics of the boards were measured about a month after the neutron irradiation, since a cooling period was needed to reach a safe dose limit. Two boards with doses of 1.2×10^{12} and 1.8×10^{12} n/cm^2 were still functioning, while two other boards with higher doses displayed very high thresholds and increased noise.

The second test involving six other boards had two parts [7]. Two months prior to the neutron irradiation, the boards were placed in the 63 MeV proton beam and a TID of 5 krad was delivered during 2.5 min. The boards were powered and the static parameters were monitored with no changes found during the exposure. The dynamic characteristics of the boards were measured after this test and compared to ones obtained before the test. The parameters of the boards were the same, confirming the results observed earlier in the separate 63 MeV proton beam test.

After the test in the proton beam, the boards were then exposed to a reactor neutron fluence up to 2×10^{12} n/cm^2 and to a TID of about 60 krad from accompanying gamma rays. The boards were powered and exposure was 14 min long. The static parameters were monitored during exposure. The board regulator power voltage and the voltages of the preamplifier and discriminator had increased by 2–5% by the end of exposure. The dynamic characteristics of the boards were measured several times after the neutron irradiation. The set of data included five measurements made at intervals of 1–2 weeks, with the first measurement taken about 40 days after the neutron irradiation. The last three tests included two periods of 1 week each and one period of 4 weeks in which the boards were heated in an oven at 110 °C. Two boards from the six were found to still be working in the first measurement. The rest came to life after 1 week of heating in the oven at 110 °C. All boards showed moderate changes in their dynamic characteristics after irradiation by neutrons. Five more weeks of heating brought the parameters of the boards closer to their values measured before the proton test [7].

From our results, we can roughly estimate that, for the test doses given above, the self-annealing time is about a few months at room temperature. Since the LHC rate of real radiation exposure is much slower than in the test, and assuming that the observed effects were cumulative, we can conclude that the anode front-end boards should not show any significant radiation damage during 10 years of normal high-luminosity LHC operation.

4. Mass production testing

4.1. Goals of the testing and the test procedures

The goals of the mass production testing of the anode front-end electronics were the following:

- assure the quality of the anode front-end electronics, which includes reliability, channel and board uniformity, and good timing performance;
- measure and certify the basic parameters of the boards;

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- produce complete documentation needed for installation checkout, commissioning, and maintenance.

A special set of test equipment, techniques, and corresponding software were developed and used to provide the following steps in the test procedure:

- selection of the preamplifier/shaper/discriminator ASICs for the AFEBs;
- test of the functionality of the assembled boards at the factory;
- an AFEB burn-in test;
- final certification tests of the AFEBs, followed by the loading of all test information into a production database;
- selection test of the controllable time delay ASICs.

About 12,200 boards were tested, with a yield of more than 90%. Similarly, we have tested about 24,000 delay chips, with a yield of 88%. Approximately 100 boards/day and 300 delay chips/day were tested by two operators. The mass production test data and results for the boards were stored in a production database [21] for detector calibration and simulation purposes, as well as for board traceability. The status of the tests and the results were monitored during the entire period of the mass production test [22]. The details of the tests and the equipment are given below.

4.2. The anode front-end electronics test steps

The first step of the test was the acceptance of the CMP16 ASICs for installation on the AD16 boards (during the microcircuit production the manufacturer tested only the quality of the wafers). The following tests were used to select good chips on the CMP16 test stand:

- measurement of the current consumption (100 mA ± 10%);
- functionality check of all 16 channels;
- measurement of critical dynamic parameters for each channel by varying the input charge.

The ASIC's threshold, noise, and propagation time must be within a given range for each parameter. Failure of any test leads to rejection of the ASIC. The yield of good chips was 92% for the total number of tested chips of ~31,200. The dominant failures were large current consumption, dead channels, and significant deviations of the threshold or propagation time in one channel.

The second test step was performed by the AFEB manufacturer (ACC Electronix, Inc., Normal, IL, USA) after the board assembly with the installed CMP16 ASIC. In addition to the high quality requirements and control of the fabrication process, the manufacturer used our test equipment and our technique to check the board functionality and assure the quality of the board assembly. This test included only a threshold measurement. The rejected boards were visually examined to find and fix most of the board assembly mistakes.

Before the final test, the assembled boards went through a burn-in procedure. The goal of the burn-in test was to increase the board reliability by detecting most of the hidden defects. During the 72-h long test at a temperature of 90 °C, the boards were powered and pulsed by a generator. The burn-in time was selected as 1% of the equivalent AFEB reliability test duration. The estimation of the AFEB reliability was made earlier by burning in 100 preproduction boards in an oven (see Section 3.3). In the mass production burn-in test of 12200 boards, only 30 boards were found to not be operational afterwards. The sole reason for these failures was bad solder contacts, which were easily fixed.

The description of the final AFEB test and its results are given in Section 4.4. The D16G delay chip test is presented in Section 4.5.

4.3. Test equipment

Four specially automated test setups [8,23] were developed and used for the mass production test. Each setup has two types of CAMAC modules: a specially designed precise pulse generator and a LeCroy 3377 TDC (standard module set), as well as a specific adapter for each setup. Three different adapters are used in the three setups for testing the

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CMP16 ASICs and the AD16 boards at different production testing stages:

- 2CMP16A—adapter for testing two CMP16 ASICs simultaneously using 2 commercial clamshell connectors (Yamaichi Electronics USA, Inc., San Jose, CA, USA);
- 2AD16A—adapter for testing two AD16 boards, used for the assembly test at the factory and for a quick test during repairs;
- 10AD16A—adapter for the final test and certification of 10 AD16 boards at once.

Each adapter receives a test pulse with a precise amplitude from the pulse generator and simultaneously injects charge into each amplifier channel through an equivalent injection capacitance of 1.6 pF. The adapter also emulates the largest detector capacitance (180 pF). Adapters 2CMP16A and 2AD16A are used in corresponding test stands equipped with one standard module set. The stand for the final test and certification of the AD16 has the 10AD16A adapter and five standard module sets. All three stands have the same general structure (Fig. 11).

The pulse generator produces a START signal for the TDC and a synchronized test pulse with a programmable precise amplitude and a rise time of 10 ns for the adapter. It also supplies power for the board and a programmable threshold voltage for the CMP16 discriminators. A specially designed 32-channel LVDS/ECL converter matches the CMP16 or AD16 LVDS standard outputs to the emitter coupled logic (ECL) standard of the TDC inputs. It is located in the pulse generator module. The LeCroy 3377 TDC (with a resolution of 0.5 ns) is used as the main DAQ module.

We checked that the simultaneous testing of all 16 channels of the AFEB gave practically the same results as when the channels were tested one by one. In the single-channel test, small systematic differences were observed for only two parameters: the noise (9% increase) and the propagation time (1 ns decrease).

The fourth test stand was designed for testing the delay chips (Fig. 12). This stand has one standard module set and its own special 2D16GA adapter with two commercial clamshell connectors to host the two D16G ASICs. The D16G test setup uses START pulses from the pulse generator to feed the 2D16GA adapter and to start the TDC. The 2D16GA adapter converts the input NIM nuclear instrumentation module (NIM) pulse to an LVDS signal and sends it to the D16G inputs. The adapter converts the D16G output pulses from transistor–transistor logic (TTL) standard to ECL for matching to the LeCroy TDC inputs. The delay chips are controlled by a PC through an LPT port (Fig. 12).

Each stand is controlled with an Adaptec 2940 SCSI PCI Adapter and a Jorway 73A CAMAC Crate Controller by a PC using a device driver [24]. The data acquisition and on-line software use

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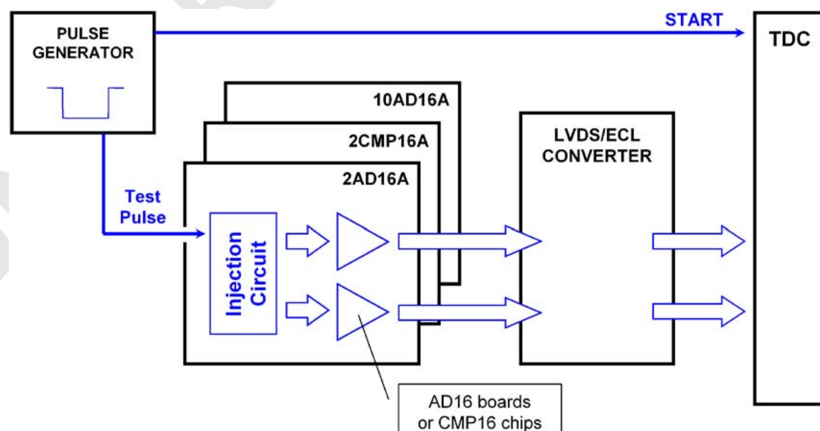

Fig. 11. Structure of the CMP16 ASIC and AD16 board test stand [8].

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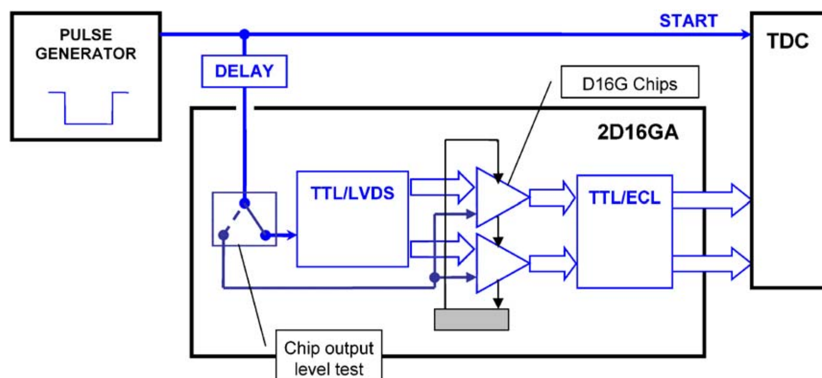

Fig. 12. D16G test stand structure [8].

Borland C++ code running in the NT Windows environment.

The sensitive analog electronics test equipment requires careful grounding. This was even more complicated because of the neighboring CAMAC electronics with the chip/board adapters. Therefore, every adapter had a carefully organized internal ground, and the ground connection between the adapter and the CAMAC modules was separately optimized for each setup.

4.4. AFEB final test and certification

The final AFEB test includes measurements of the following characteristics for each AFEB channel: threshold, noise, gain, discriminator offset, time resolution, propagation time, slewing time, and internal test capacitance. The DAQ interface of the test stand allows the operator to set all the conditions of the test: the minimum amplitude of the test signal, the amplitude increment, the number of steps, and the number of input pulses at each amplitude. The number of pulses recorded by the TDC for each value of the amplitude is used to obtain the threshold curve. The mean and RMS of the TDC time distribution for each amplitude of the input pulse give the propagation time and the time resolution, respectively.

Each board is measured four times at different conditions, providing four sets of data: three threshold measurements and one timing measurement. The first two sets of threshold measurements have two different discriminator threshold settings U_{set} of 150 and 300 mV. They are taken with the test pulse going through the injection circuits of the adapter and the signal inputs of the board. The test pulse amplitude is varied around the ASIC thresholds. These data are used to get the corresponding threshold Q_{thr} and the noise in terms of the input charge, as well as the preamplifier gain and the discriminator offset. The input charge Q_{in} was defined as the maximum of the test pulse amplitude multiplied by the nominal value of 1.6 pF for the injection capacitance. The negative test pulse had a rise time of ~10 ns. The gain and offset were obtained with the use of the threshold Q_{thr} versus discriminator threshold setting U_{set} and the linear approximation $Q_{thr} * \text{Gain} = \text{Offset} + U_{set}$.

In the third set of conditions, the discriminator setting is still 150 mV, but the test pulse feeds each CMP16 ASIC channel through its own internal capacitance, with a nominal value of 0.25 pF. The technological variation of this capacitor can be up to 20% of its nominal value. The real value of each internal capacitor is calculated by multiplying the nominal value of 0.25 pF by the ratio of the Q_{thr} in the first set to the Q_{thr} obtained in the third set. The measurement of the internal capacitance is an important issue because the use of this capacitance provides the only possible threshold calibration test for the board when it is installed on the

chamber and fired by the test pulse from the ALCT.

The timing parameters of the boards are measured in the fourth set of data taken at the same conditions as in the first threshold measurement. However, the amplitude of the test signal is varied through the full scale of the pulse generator (equivalent to a Q_{in} of up to 600 fC). The results are the resolution and propagation time dependencies versus the input charge. The slewing time is measured in an off-line analysis as the difference between the maximum and minimum values of the propagation time observed in the region from approximately 2–20 times the threshold at a discriminator setting of 150 mV.

The on-line analysis of the data allows us to display and to check promptly the coarse values of the basic board parameters, such as threshold, noise, and propagation time, against their allowed limits, providing the first level of board rejection. An example of the on-line display test results for the threshold and noise is given in Fig. 13. The value of the tested parameter for each channel is presented as a colored bar. If a parameter is out of limits, the corresponding bar becomes red, signaling the problem to the operator.

The data for the boards that pass the on-line criteria are analyzed off-line with the use of the ROOT [25] based program, where the final values of all parameters for each board are calculated. For example, the threshold curve is fitted by a cumulative distribution function, which includes a Gaussian error function with two free parameters: a mean as the threshold Q_{thr} and a standard deviation as the noise (Fig. 14). There were 400 test input pulses at each amplitude. The fit procedure was very stable for all the tested boards and the mean of the reduced χ^2 distribution was 1.07. The reduced χ^2, along with other selection criteria, were used in determining which boards passed our tests.

The results for each board are filtered through the set of certification cuts [22]. The cuts impose limits on the average values of each parameter and on the maximum deviation of each channel's parameter from the board average in order to assure good uniformity of the parameters within a board. For the noise, time resolution, and slewing time, instead of the maximum deviation, we used the maximum value of each parameter. As an example, the distributions of the threshold and noise for all certified boards from the first set of measurements are presented in Fig. 15 and Fig. 16, respectively. The distributions of the propagation time and slewing time from the fourth set of data are shown in Figs. 17 and 18 [22].

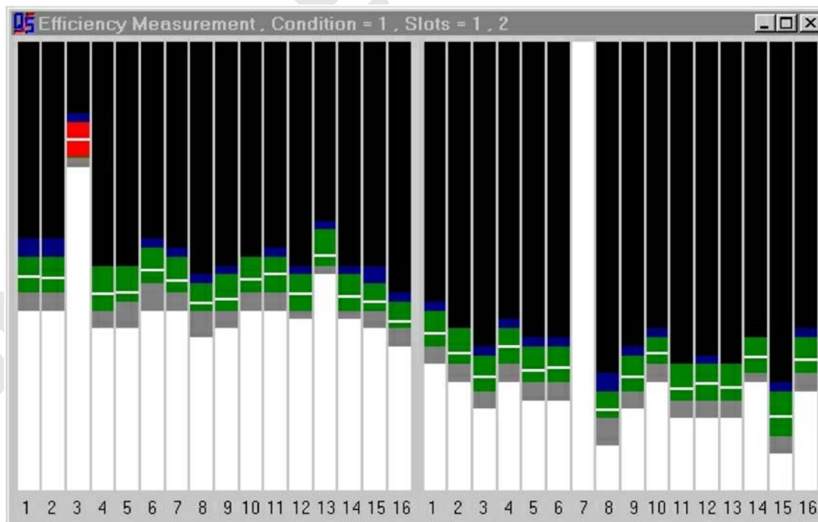

Fig. 13. AD16 board test stand display showing the measured threshold for each channel on two boards [8]. Channel 3 of board 1 has a large threshold deviation and channel 7 of board 2 is dead.

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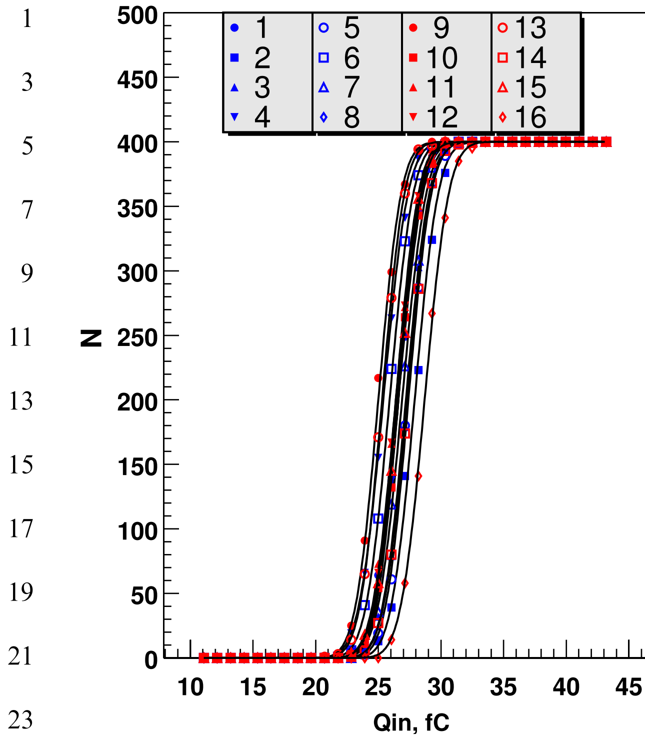

Fig. 14. Threshold characteristics for all 16 channels of an AFEB. The solid lines show the fitted functions.

While the uniformity of the channel parameters within a chip was expected to be rather high (a typical feature of integrated circuits), the average parameters of the CMP16 ASICs itself might have significant variations from chip to chip due to different positions of the circuit on the silicon wafer and differences between the wafers during the mass production of the CMP16 ASICs. However, the results of the mass production test show that the spread of the characteristics from chip to chip is small and well within the acceptable limits for the vast majority of the boards. The overall yield of good boards was about 92%. Most of the failed boards did not pass one or two selection criteria. The most frequent failures were a high minimal threshold ($Q_{thr} > 15$ fC at $U_{set} = 0$) and a spread of the propagation time for a low input signal of 50 fC and a threshold of about 30 fC outside the limits. These boards were repaired by tuning the discriminator current and other controls. Only ~1.3% of the boards from 12,200 had their CMP16 ASICs replaced.

Table 3 presents a summary of the parameters for the certified AD16 boards. All parameters, except the gain and offset, were obtained with a discriminator threshold setting of 150 mV. The first column gives the mean value and standard deviation (RMS) of the distribution for each

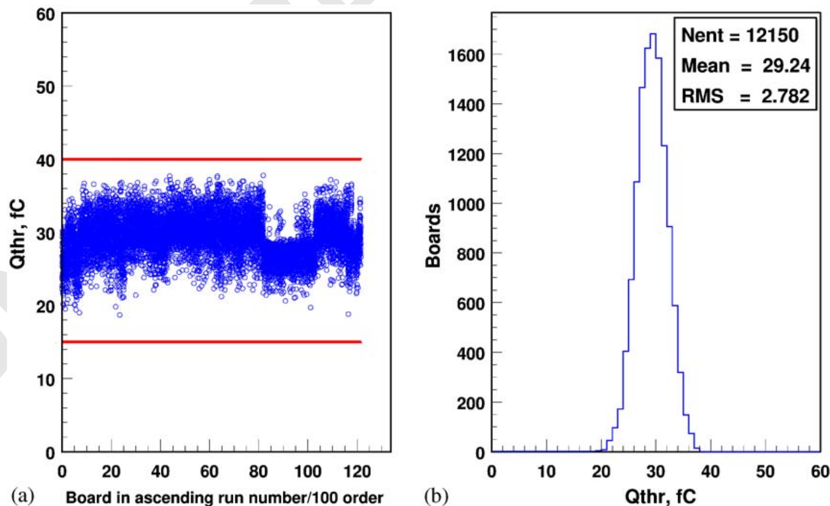

Fig. 15. (a) Average threshold Q_{thr}vs. board number. The solid lines show the threshold acceptance limits. (b). Histogram of the average board thresholds Q_{thr}.

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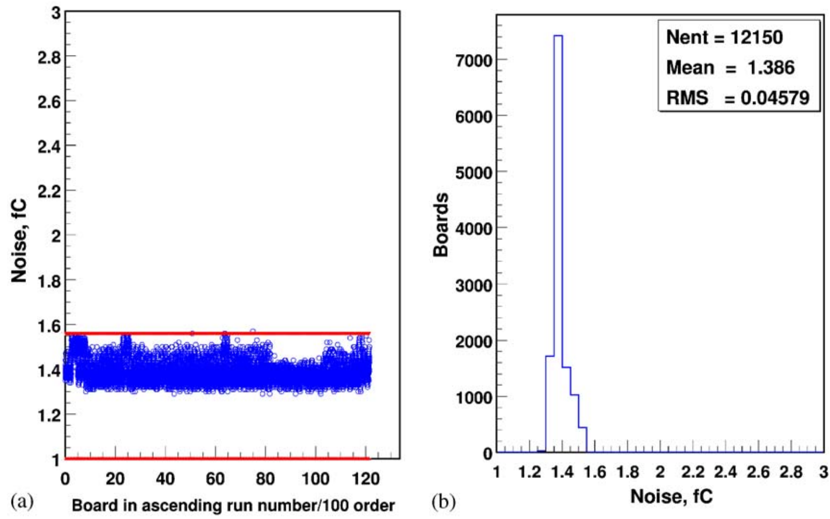

Fig. 16. (a) Average noise vs. board number. The solid line shows the acceptance upper limit. (b). Average board noise distribution.

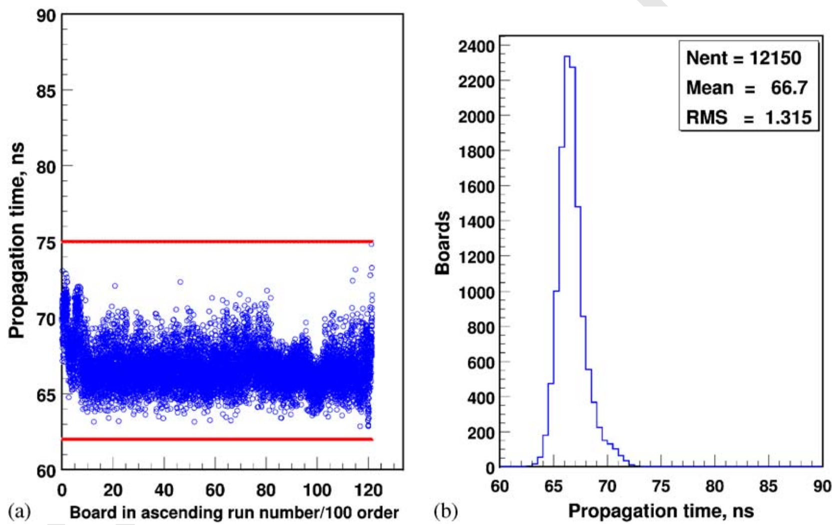

Fig. 17. (a) Average propagation time vs. board number. The solid lines show the acceptance limits. (b). Distribution of the average board propagation time.

parameter, averaged over all the channels of the board. Note that the average threshold and average propagation time are controlled parameters. The results in the first column do not include any systematic errors, which are on the order of 10%. The actual average slewing time is higher by about 0.6 ns from the measured AFEB slewing time of 2.4 ns due to the contribution of the pulse generator's intrinsic slewing time. Because the START signal for the TDC comes from the generator (Fig. 11) and the STOP signal from the AD16 board, the slewing time of the generator partially compensates for the slewing time of the CMP16 chip on AD16 board, and thus must be taken out of the chip slewing time calculation. The uniformity of the channels within each board is

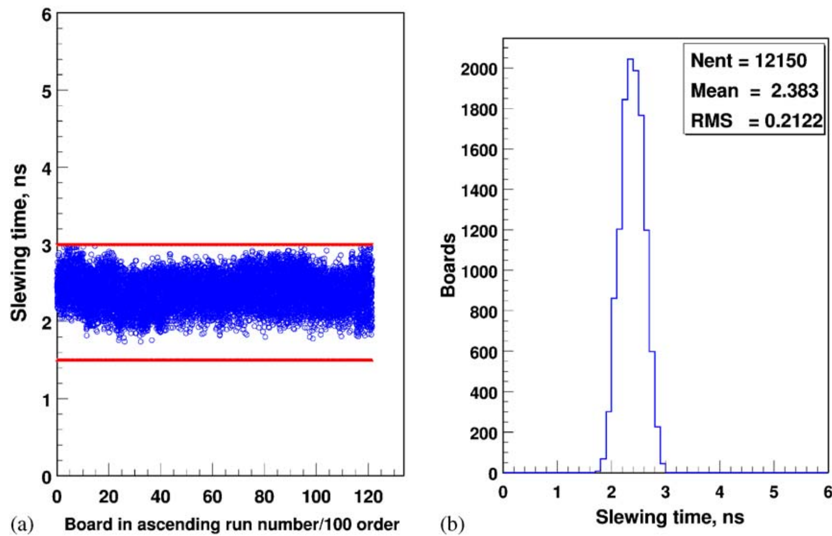

Fig. 18. (a) Average slewing time vs. board number. The solid lines show the acceptance limits. (b) Distribution of the average board slewing time.

Table 3
Summary of the measured parameters for the certified AD16 boards

Parameter	Average ± RMS	Uniformity (RMS)
Threshold (fC)	29.2 ± 2.8	0.9
Noise (fC) at $C_{det} = 180$ pF	1.4 ± 0.05	0.05
Transfer function (gain, mV/fC)	6.9 ± 0.3	0.07
Discriminator offset (mV)	51 ± 19	6
CMP16 internal capacitance (pF)	0.24 ± 0.02	0.01
Propagation time (ns) at $Q_{in} = 100$ fC	66.7 ± 1.3	0.3
Resolution time (ns) at $Q_{in} = 100$ fC	0.6 ± 0.04	0.06
Slewing time (ns) for $Q_{in} = 60$–600 fC	2.4 ± 0.2	0.2

characterized in the second column as the standard deviation (RMS) of the channel residual, defined as the difference between the channel parameter and its value averaged over the 16 channels of each board.

The stability of the AFEB test stand was monitored throughout the 1 year of testing, with data taken each day using the same set of 10 boards assigned to each of the 10 slots of the 10AD16A adapter. The largest changes seen were in the slewing time for the monitoring boards, shown in Fig. 19. The variations did not exceed ±0.4 ns.

All raw data, test conditions, calibration constants, and results of the off-line analysis were stored in a production database. This is an Oracle application [21], installed on the central CERN Oracle database. The data are used for documentation and checking purposes by the CMS CSC Final Assembly and System Testing (FAST) sites in the USA, Russia, and China. They will also be important during CMS maintenance and operation. The data are accessible through a Web connection using the Oracle9i Application Server and PL/SQL procedures.

4.5. D16G delay chip selection

The delay chip test stand measures the propagation time of the chips. The propagation time is controlled by the delay code, which varies from 0–15 with an average delay step of ~2 ns. The test also checks the test level feature of the chips. The selection of good delay chips is made on-line using the test stand. Chips having dead channels or

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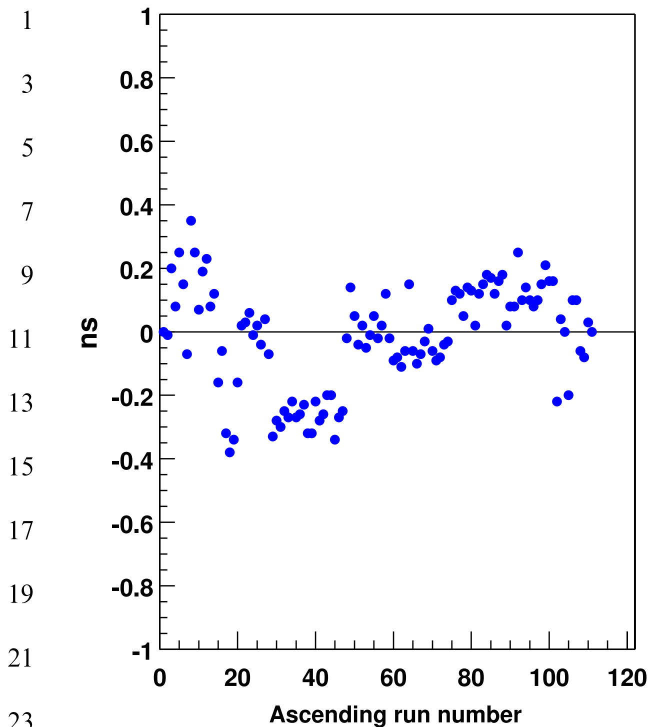

Fig. 19. Change in the average slewing time relative to the beginning value vs. run number for the monitoring board in slot 9 of the 10AD16A adapter.

faulty control of the delay step or the test level are rejected without any further on-line analysis. Parameters of the functional chips are checked against a list of acceptance criteria. The most important are the delay uniformity across the 16 channels of the chip at each delay code and the linearity of the delay versus code dependence. The main problem with the delay chip test stand was a degradation of the contacts of the commercial clamshell connectors. The connectors were replaced regularly after approximately 3000 connections.

A total of about 23,700 delay chips were tested, with a yield of accepted chips of 88%. Due to the technological spread of the average delay step, the accepted chips were divided into nine separate groups, each having a 2 ns wide bin in the distribution of the average chip delay at a delay code of 15 (see Fig. 20). Groups from five to eight (78% of the accepted chips) were used for the ALCT board production, with chips from the same group always being used on any ALCT board.

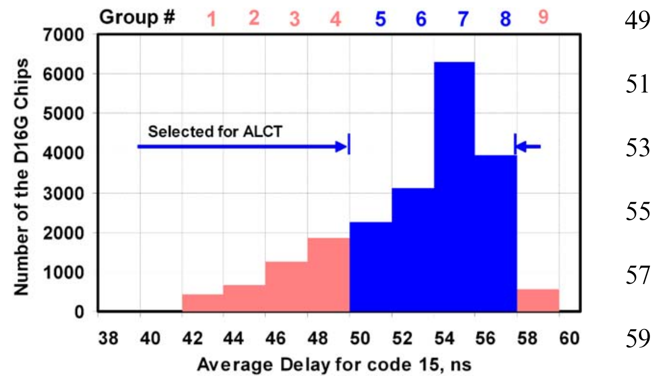

Fig. 20. Distribution of the average time delay for the delay chips, showing the division by groups [8].

4.6. Testing at CSC assembly sites

Extensive tests of the anode front-end electronics were performed at the FAST sites at the University of Florida, UCLA (USA), PNPI (Russia), and IHEP (China) [15]. These tests are part of the complete set of tests of the chambers after they have been fully equipped with the anode and cathode front-end electronics at the FAST site. For the anode electronics the list of tests includes the following:

- measurement of the background rates at a CSC high voltage of 3.6 kV and 3.8 kV;
- connectivity and crosstalk tests;
- measurement of the thresholds and analog noise;
- measurements of the time delays;
- a high statistics cosmic ray test and a high voltage plateau measurement.

Similar tests take place at CERN [26] after chambers from the FAST sites arrive at CERN. The results of all tests confirm the high performance of the anode front-end electronics [27]. The characteristics of the electronics measured in the independent tests at the FAST sites are consistent with the parameters obtained in the mass production tests using the test stands.

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5. Conclusions

The anode front-end electronics of the CMS Endcap Muon CSCs have been produced and have successfully passed the mass production tests. The characteristics of the anode front-end boards AD16 and delay chips D16G satisfy the baseline goals and confirm the performance expectations based on the experience with the pre-production samples.

A specialized set of test equipment, techniques, and corresponding software have been developed and used for the mass production tests. The data and results have been stored in a central Oracle database at CERN for use during maintenance and operation of the CMS experiment.

Acknowledgments

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