Anode Front-End Electronics for the Cathode Strip Chambers of the CMS Endcap Muon Detector

N. Bondar*a), T. Ferguson**, A. Golyash*, V. Sedov*, N. Terentiev**.

*) Petersburg Nuclear Physics Institute, Gatchina, 188350, Russia
**) Carnegie Mellon University , Pittsburgh, PA, 15213, USA
a) bondar@fnal.gov

Abstract

The front-end electronics system for the anode signals of the CMS Endcap Muon Cathode Strip Chambers has been designed. Each electronics channel consists of an input protection network, amplifier, shaper, constant-fraction discriminator, and a programmable delay with an output pulse width shaper. The essential part of the electronics is an ASIC consisting of a 16-channel amplifier-shaper-discriminator (CMP16). The ASIC was optimized for the large cathode chamber size of up to 3.4 x 1.5 m^2 and for the large input capacitance (up to 200 pF). The ASIC combines low power consumption (30 mW/channel) with excellent time resolution (~2 ns). The second ASIC provides a programmable time delay which allows the alignment of signals with an accuracy of 2.5 ns. The pre-production samples of the anode front–end boards with CMP16 chips have been successfully tested and the mass production has begun.

I. INTRODUCTION

The purpose of the anode front-end electronics described in this paper is to receive and prepare the anode wire signals of the Cathode Strip Chamber (CSC) of the CMS Endcap Muon (EMU) system for further logical processing in order to find the location of charged particle with a time accuracy of one bunch crossing (25 ns) [1].

Special features of the CSC are a six-plane two-coordinate measuring proportional chamber, a large chamber size (the largest one is 3.4 x 1.5 m^2) and a large detector capacitance (up to 200pF), created by joined together anode wires. Expected anode signal rate is about 20 kHz/channel. Total number of anode channels is more than 150000. The electronics is spread over the EMU detector with limited maintenance access. Estimated radiation dosage integrated over 10 LHC years is about 1.8 kRad for ionizing particles and about 10^{12} neutrons per cm^2 [1].

The electronics must satisfy the following requirements:

-Able to determine the timing of the track hit with an accuracy of one bunch crossing with a high efficiency;

-Match the chamber features to achieve optimal detector performance.

-Be reliable during for 10 LHC years

-Have sufficient radiation hardness

-Have low power consumption [1].

II. ANODE ELECTRONICS STRUCTURE

A. Anode electronics specification

To achieve accordance between a large detector size and a large detector capacitance on one hand and high sensitivity and time accuracy on the other hand, a relatively large shaping time of 30 ns for the anode signals, together with two-threshold constant-fraction discriminator, were proposed. This shaping time allows us to collect about 12% of the initial charge. Together with the discriminator threshold as low as 20 fC, the efficiency plateau starts at 3.4kV [2]. The nominal operating point of the chamber is set at 3.6 kV and the average collected anode charge is about 140 fC.

To achieve a minimum stable threshold level of anode electronics as low as 20 fC with the minimum possible cross-talk, a standard structure of the anode electronics channel was split into three parts located on three different boards. See Figure 1 for reference. Also, the amplifier-chamber signal connection and the chamber grounding and shielding were carefully planned and executed.

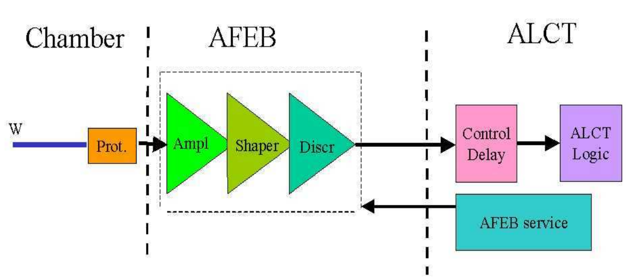

Figure 1: Anode electronics structure. Protection board (Prot.) is a part of the chamber assembly, AFEB - Anode Front-End Board is a 16-channel board, ALCT –Anode Local Charge Track finder logic board.

Two 16-channel ASICs were designed to produce the anode structure. The first one is a 16-channel amplifier-shaper- discriminator with an LVDS driver for output signals, named CMP16, and the second one is an LVDS-receiver - control-delay - pulse-width-shaper, named DEL16. This solution allows us to simplify the electronics board and increase the electronics reliability and maintainability, as well as minimise power consumption. Standard BiCMOS and CMOS technologies were used for designing the ASICs, giving us a relatively low price and sufficient radiation hardness.

B. *Chamber ground and shielding. Protection Board.*

The chamber anode wires, cathode planes, protection boards and even the cathode amplifier input connections are all parts of the anode amplifier input circuit. To obtain optimal performance of the chamber, we have to observe the following rules: The anode amplifier input impedance must be close to the anode wire structure characteristic impedance (~50 Ohm). The cathode input impedance must be close to the characteristic impedance of the cathode strip structure. The detector-amplifier ground connection should be as short as possible and as wide as possible in order to have the minimum possible inductance for the connection [3].

Each chamber plane has a solid metal cathode plate. This plate is a natural chamber signal ground for the plane. Both anode and cathode amplifiers input ground terminals are connected to this plane. The chamber's outer copper foil along with the chamber metal frame and side covers create the detector RF case. The RF case and the signal ground are connected together at the amplifier side of the chamber to avoid a ground loop through the signal ground plate and along the amplifier input ground circuit.

The protection board (PB) has two functions. The first one is to fan-in the chamber anode signals and adapt them to a standard 34-pin connector. The protection board collects signals from two chamber planes (8+8) and provides a proper ground connection between the chamber signal ground and the amplifier input ground The second function of the PB is to protect the inputs of the amplifier against accidental sparks in the chamber. The full protection network consists of two resistor-diode stages. The first protection stage is placed on the protection board in order to minimize the emergency current loop for better protection, and the second stage is on the input of the anode front-end board.

C. *Anode Front-End Board (AFEB)*

On the basis of the CMP16 chip, the 16-channel Anode Front-End Board (AFEB) AD16 is designed. This board receives the anode signals from the chamber wire groups, amplifies the signals, selects the signals over the preset threshold with precise time accuracy and transmits the logic level signals to the further stage with the LVDS levels standard. Since the EMU system contains almost 10,000 AD16 boards, we have designed the AFEB in the simplest and cheapest way. There is only one CMP16 chip with the necessary minimum service components on it as well as a small voltage regulator to keep the "on-board voltage" stable, well filtered and independent of the power supply voltage. The board has a 34-pin input connector and a 40-pin output connector. Normally, this board is connected to the chamber's protection board and fixed on the chamber side cover with a special bracket, providing a reliable and proper junction. A 20-pair twisted-pair cable connects the AFEB with the ALCT board. Since the functions to serve the AFEB are delegated to the ALCT board, this cable is used both to transmit output signals to the ALCT and to supply the board with power voltage, threshold voltage and test pulses. The DEL16 ASIC is a signal receiver at the very input of the ALCT .The ALCT provides the following AFEB services: a power supply voltage distribution circuit, a "power-ON/OFF" command driver for each AFEB, a threshold voltage source for each AFEB and a few test pulse generators to test the AFEB through its internal capacitance or through a special test strip on the cathode plane to inject input charge directly onto the anode wires [4].

III. Amplifier ASIC CMP16

The main component of the AFEB is an amplifier-discriminator ASIC. The chip parameters are specially optimized for the Endcap EMU CSC to obtain optimal performance from the chamber. The ASIC has the following electrical characteristics:

Input impedance	40 Ohm
Transfer function	7 mV/fC
Shaper peaking time	30 ns
Shaped waveform	Semi-gaussian with Two-exponent tail cancellation
Amplifier input noise	0.5 fC @Cin=0
	1.7 fC @Cin=200 pF
Non-linearity	<10%; 0-1.5 V
Two-threshold discriminator	High threshold used as ENABLE
Low-threshold zero-crossing discriminator driven by constant-fraction shaped pulse.	
High-level threshold	adjustable 0 - 100 fC
Discriminator slewing time	3 ns
Power supply voltage	5 V
Power consumption	0.5 W/chip

The schematic diagram of one amplifier-discriminator channel is presented in Figure 2.

The amplifier-discriminator-shaper chip based on these specifications was designed using a BiCMOS 1.5 micron technology and was made at the AMI foundry through the MOSIS Service. One chip contains 16 identical channels and one special test channel. Each channel has a test capacitor (~0.25 pF) connected to the input node of the amplifier. The chip package is a plastic 80-pin Quad Flat Pack with a pin pitch of 0.8 mm. The chip size is 14 x 20 mm^2.

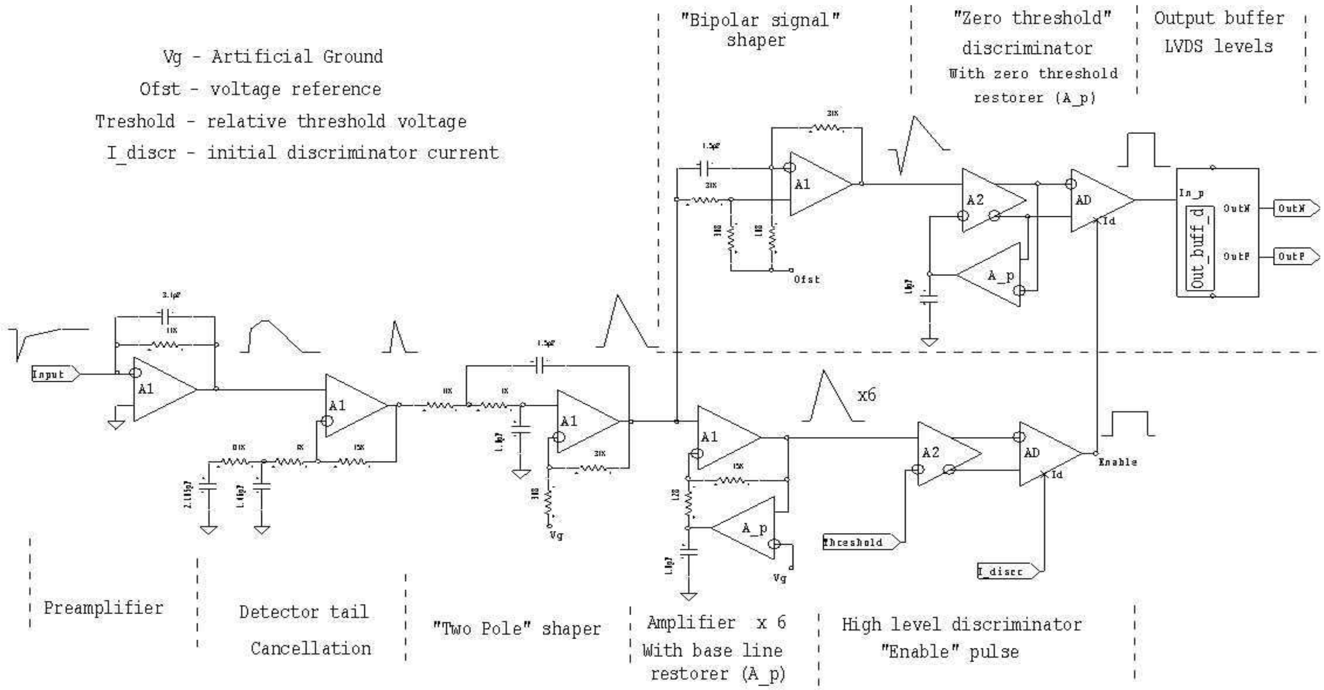

Figure 2: Schematic diagram of an anode amplifier-discriminator channel.

IV. DELAY ASIC DEL16

The anode pulses to the ALCT have a big variation of phase for various reasons, including different length of cables to the input of ALCT. The total time variation may be up to 20 ns. To align the input pulse phases, a special 16-channel control delay chip was designed. The structure of one channel of this chip is presented in Figure 3. Each channel consists of an input LVDS-to-CMOS level converter; four stages of delay with 1, 2, 4, and 8 steps; an output width pulse shaper. Also, the chip has the possibility to generate a test level at each output. This option is used for testing chip-to-chip connections. The chip has a serial interface to control the delay and set the output test level.

Delay channel parameters:

Input signal level LVDS standard

Output signal	3.3 V CMOS
Minimum delay	20 ns
Delay step	2 ns (adjustable with an external current)
Delay steps	15 maximum
Delay nonlinearity	+/- 1 ns
Output pulse width	40 ns (adjustable with an external current)
Power supply voltage	3.3 V
Power consumption	0.2 W

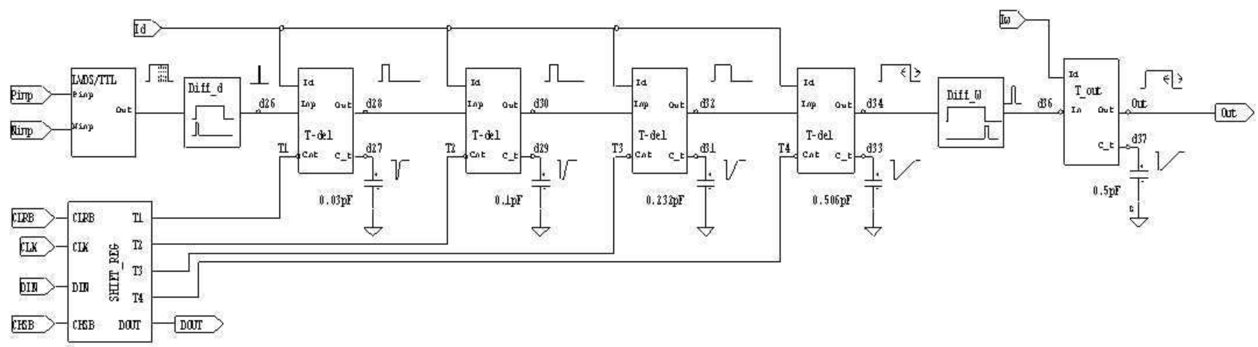

Figure 3: Schematic diagram of one delay channel

The chip was designed using the AMI CMOS 0.5-micron technology. The chip was made in the AMI foundry via the MOSIS Service. The chip is packaged in a plastic 64-pin Quad Flat Pack with a pin pitch of 0.5 mm. The chip size is 10 x 10 mm^2.

V. ANODE ELECTRONICS TEST

A. Chamber performance

The CSC with the anode electronics has been tested on the Cosmic Muon Stand at FNAL. We have reached a minimum discriminator threshold for the anode electronics installed on the chamber as low as 10 fC. We assume that 20 fC threshold is a normal operational value. A standard CSC in that case has an efficiency plateau with a gas mixture of $Ar+CO_2+CF_4$=40+50+10, starting at 3.4 kV.

A full-scale prototype CSC, completely equipped with electronics, was tested in a beam at CERN at the Gamma Irradiation Facility. The CSC performance was within the baseline requirements. In Figure 4, the final result of the bunch tagging efficiency is shown [2].

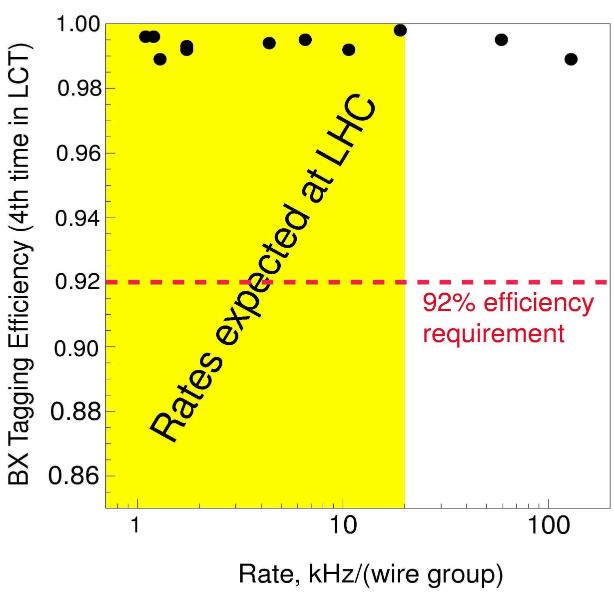

Figure 4: Bunch crossing tagging efficiency (in 25 ns gate) vs GIF rate.

B. Reliability test

To measure the reliability of the AFEB AD16, we put 100 AD16 boards (1,600 amplifier-discriminator channels) into an oven at a temperature of 110^{O}C. We assume that for each 20 degrees the failure rate increases about two. The boards were supplied with power and the thresholds on the boards were set to minimum to start self-oscillation. Total test time in the oven was 4000 hours. This time corresponds to about 7 years of real operation at 30^{O}C. Every two weeks we measured the board parameters. During the test, we have no failures and there were no visible changes in the electrical characteristics.

C. Radiation test

Since the AFEB contains both BiCMOS and bipolar components we had to test the Total Ionizing Dose (TID), Displacement and Single Effect Event (SEE) damages. [3] A few samples of the AFEB were irradiated with a 63 MeV proton beam at the University of California, Davis to test the electronics for TID and SEE damages. No latch-up or spikes or any changes in the static parameters were observed. At the required TID level of 5-6 kRad all changes of gain and slewing time were practically negligible [5].

To test the electronics for possible Displacement damages the same boards were irradiated with 1 MeV neutrons from a reactor at Ohio State University. Total neutron fluence up to 2×10^{12} n/cm^2 was accompanied with a significant γ flux. The boards also received a TID of 50-60 kRad. Two boards were found working 40 days after the irradiation and others after one week of heating in an oven at 100^{O} C [5].

D. AFEB mass production test

A special automated test setup and test methods has been developed to measure the CMP16 chip and the AD16 board parameters, as well as delay chip DEL16 parameters. The test stand schematic structure is illustrated in Figure 5.

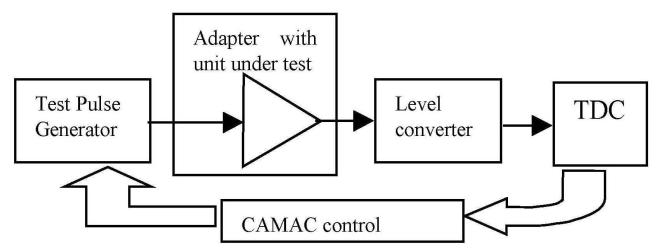

Figure 5: Test stand block structure.

There is a specially designed pulse generator for producing test pulses with the necessary accuracy and shape. The second main unit is a LeCroy 3377 TDC. We have designed three special adapters to match the different devices to be tested with the test setup.

We use the following procedure for testing the parameters of the AFEB: Discriminator threshold is set at one of two standard levels, about 20 or 40 fC. The input pulse amplitude is increased in steps to supply the amplifiers with an input charge from 0 fC to 100 fC for threshold testing and from 0 fC to 500 fC for time slewing testing. The generator sends 400 pulses at each step. The TDC measures the number of AFEB's output pulses and propagation time of the CMP16 versus the amplitude of the input signal. The resulting curves of "output pulse count versus input amplitude" for two different thresholds (threshold test) are used to derive the required CMP16 parameters. Amplifier noise is calculated from the curve slope. For the amplifier gain calculation and getting threshold calibration, we use two curves, one at 150 mV threshold voltage, and the second at 400 mV. The resulting curve of "propagation time versus input amplitude" (timing test) is used to estimate the CMP16 slewing time.

We use a multi-step test procedure for AFEB verification. The first step is a selection of good chips for assembly on the board. A special clamp-shell adapter for two chips is used. The chip under test has normal power voltage of 5V, threshold voltage of 150 mV (about 20 fC of input charge); the amplifier input capacitor of 0 pF. The test pulse amplitude is ramped up to provide an input charge through the chip's internal capacitance from 0 fC to 200 fC. A good chip must satisfy the following requirements: a noise level less than 0.8 fC @ Cin=0 pF; a threshold uniformity better than +/-10%; a deviation of propagation time should be within 4ns for all channels of the chip for input signals from 50 fC to 200 fC.

The assembly company performs a test on the assembled board according to our test procedure and using our equipment.

All assembled boards are put through a burn-in procedure. We keep the boards for 75 hours in an oven at 100 C with the power on and with an input test pulse. After the burn-in procedure, all boards are given a final test, calibration and certification.

A special adapter for testing and calibrating boards was designed. The adapter has a special injection circuit and 200 pF input capacitance for each amplifier's input. Injection circuit accuracy is better than 2% after calibration. The final test and calibration procedure has four test runs with the following conditions:

1 -low threshold, external injection circuit,

2 -high threshold, external injection circuit,

3 -low threshold, the chip internal capacitance as an injection circuit,

4 -low threshold, time measurement.

The following parameters are collected from the data:

- Threshold level as a function of threshold voltage,
- Threshold uniformity for each chip,
- Noise level at Cin=200 pF,
- Propagation time as a function of the input signal amplitude,
- Propagation time uniformity,
- Chip time resolution,
- Chip's internal test injection capacitance.

The raw test data and the final results are stored in a database. We intend to keep the board calibration and certification results in a database for further experimental needs

E. Delay chip mass production test

A special clamp-shell adapter for two chips was designed in order to use the existing test setup for delay chip testing. The following test procedure is used: The test program scans the delay code in the DEL16 chip in steps of "one" from delay code "0" to the maximum delay code "15". The test generator sends 100 input pulses for each delay step, and the propagation time for each step is measured by the TDC. The output test level generating option is measure by switching-on this option for each channel and measuring the chip output voltage for that channel.

A good chip must satisfy the following conditions: the control interface can switch on a test level at the chip outputs, the maximum delay and output pulse width should meet the specifications, and the delay step variation between channels must be less than half of the delay step.

VI. CONCLUSION

The anode front-end electronics for the Endcap Muon CSC and the electronics layout on the chamber were carefully designed and arranged to obtain the best chamber performance. The CSC test results show us that the chamber equipped with the electronics meets the baseline requirements.

Special equipment and necessary procedures were designed for testing and calibrating the electronics at every stage of the mass production and the CSC final assembly. The electronics calibration and test results will be available for the duration of the experiment.

The electronics mass production has started.

VII. REFERENCES

1. CMS The Muon Project Technical Design Report CERN/LHCC 97-32 CMS TDR 3 1997.

2. D. Acosta et al, "Large CMS Cathode Strip Chambers: design and performance." Nucl. Instrum. Meth. A453:182-187, 2000.

3. N. Bondar, "Design of the Analog Electronics for the Anodes of the Proportional Chambers for the Muon Detector of the GEM Unit" Preprint EP-3-1994-1945, PNPI, 1994.

4. J. Hauser et al, "Wire LCT Card" at http://www-collider.physics.ucla.edu/cms/trigger/wirelct.html.

5. T. Ferguson, N. Terentiev, N. Bondar, A. Golyash, V. Sedov "Results of Radiation Tests of the Anode Front-End Boards for the CMS End-Cap Muon Cathode Strip Chambers", in these proceedings.