Anode Front-End electronics status.

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Anode Front-End electronics status

- AFEB production status
  - -CMP16-G ASIC
  - -AFEB production
  - -AFEB certification
  - -AFEB shipment
- Documentation
- AFEB-ALCT cable production
- Delay chip DEL16 test status
- ME 234/2 HV noise investigation

AFEB production status

16 Cannel Amplifier-Discriminator

CMP16_G

General Description

The CMP16_G is a custom designed 16 channel Amplifier-Discriminator for anode signal of proportional chambers. The circuit optimized for detector capacitance up to 200 pF and detector size up to 1.5 x 3.4 m^2. The ASIC combines low power consumption (30 mW/channel) with excellent time resolution (~2 ns). The CMP16_G is designed and fabricate using a BiCMOS 1.5 micron technology.
The chip is capsulated into a QFP-80L 14X20 plastic package.
This ASIC is designed as a part of for the anode front-end electronics for Cathode Strip Chambers of the Muon System of CMS experiment.

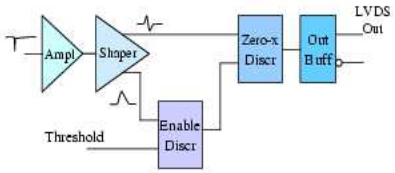
Features

Input impedance	40 Ohm
Shaper peaking time	30 ns
Shaped waveform Semi-gaussian with Two-exponent tail cancellation	
Two level constant fraction discriminator	
Discriminator slewing time	3 ns
Low power output buffer	
Output signal LVDS compatible	1.5 mA
Power supply voltage	5 V
Power consumption	0.5 W/chip
Output signal	LVDS standard

Top View

Size: 14 mm x 20 mm x 2 mm
Pin pitch: 0.8 mm.

Block Diagram



CMU-PNPI

http://www-hep.phys.cmu.edu/cms/
http://dbserv.pnpi.spb.ru/ofve/ted/

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CMP16_G ASIC

- Produced quantity 28,000
- Tested 25,000
- Assembled at USA 12,200
  sent to Dubna 1,472
- Stored on shelf 11,228

- Yield rate 90%

We have to test more 3,000 more chips.

Prepared CMP16_G Datasheet

AFEB production status

Production completed

Need to produce	12,000
Total ordered	12,200
Total delivered to FNAL	12,200

Testing completed

Certification statistic:	Total measured	12,200
	Total certified	12,160
	Yield rate after cuts	99.6%
Final yield rate (including chip selection)		~90%

Shipping completed

UCLA	2027
UF	2031
PNPI	2160
IHEP/p	1584
IHEP/s	1427
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TOTAL	9229

Detail information on the following WEB page:
http://www-hep.phys.cmu.edu/cms/MASSPRTEST/AFEB/passmp.html

Anode electronics assembly instructions.

The following instructions and manuals were prepared and located at the following WEB site http://www-hep.phys.cmu.edu/cms/ :

AFEB AD16_F user manual
Instruction for AFEB installation
Instruction for AFEB-ALCT cables installation for ME234/2 chamber
Instruction for AFEB-ALCT cables installation for ME1/2 chamber
Instruction for AFEB-ALCT cables installation for ME2/1 chamber
Instruction for AFEB-ALCT cables installation for ME3/1 chamber
Instruction for repair broken M4 thread .
Instruction for AFEB-ALCT cables installation for ME4/1 chamber
Instruction for AFEB-ALCT cables installation for ME1/3 chamber
CMP15_G Datasheet
DEL16 Datasheet
Protection board PB Datasheet

AFEB-ALCT cables status

Total cables to produce	-	10760
Total produced cables	-	9336
Production balance (ME4/1 included)	-	1424
Production balance (spare cables only)	-	92

ME234/2 - 148 sets made, shipped to US FAST sites
ME2/1 - 38 sets made, shipped to PNPI
ME3/1 - 38 sets made, ready for shipment to PNPI
ME1/2 - 74 sets made, shipped to IHEP
ME1/3 - 74 sets made, ready for shipment to IHEP
Spare - 120 cables made

Delay chip D16 status.

16 Channel Programmable Delay

D16G

General Description

The D16G is a custom designed 16-channel programmable delay circuit. Each channel consists of an input LVDS-to-CMOS level converter, four stages of delay with 1, 2, 4, and 8 steps; and output width pulse shaper. Also, the chip has the possibility to generate a test level at each output. This option is used for testing chip-to-chip connections. The chip has a serial interface to control the delay and set the output test level.

The D16G is designed and fabricated using a CMOS 0.5 micron technology.

The chip is capsulated into a QFP-64L 10X10 plastic package.

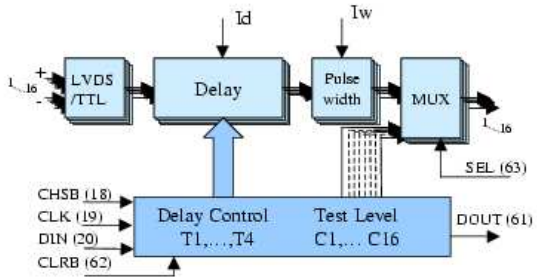
This ASIC is designed as a part of the anode front-end electronics for Cathode Strip Chambers of the Endcap of the Muon System of CMS experiment.

Features

Input signal level	LVDS standard
Input resistance	110 Ohm
Output signal	3.3 V CMOS
Number of delay steps	15
Delay step (slope)	1- 4 ns (adjustable with an external current)
Output pulse width	40 ns (adjustable with an external current)
Power supply voltage	3.3 V
Power consumption	0.2 W
Temperature drift	0.6 ns/10°C

Block Diagram

Top View



Size: 10 mm x 10 mm x 1 mm.
Pin pitch: 0.5 mm.

CMU-PNPI 1

http://www-hep.phys.cmu.edu/cms/
http://dbserv.pnpi.spb.ru/ofve/ted/

Produced	23,700
Tested	23,700
Good chips	20,811
Rejected	2,890
Yield rate (pass all cuts)	~ 88%
Spare (groups 1-4, 9)	4,873
Sent to UCLA (groups 5-8)	15,938

Prepared D16 delay chip Datasheet

Detail information on the following WEB page:

http://www-hep.phys.cmu.edu/cms/MASSPRTEST/D16GMP/passmp.html.