# Anode Electronics Calibration Results

**US CMS EMU meeting**
**Fermilab**

**November 19-21, 1999**

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## Introduction

- List of traditional measurements on ASIC stand at Fermilab:
  - Thresholds (Qth, fC) at 2-3 JTAGs
  - Noise ($\sigma$, fC) at Cdet=0 pF, 200 pF
  - Preamplifier gain, discriminator offset
  - Time resolution
  - Slewing time, delays
  - All chips in use were tested, results on CMU Web page http://www-hep.phys.cmu.edu/cms/
- All above is now available for anode front end installed on CSC:
  - test pulse thru injection boards
  - test thru cathode test strip
  - implemented in DAQ at Fermilab and in the CERN 99 test beam run (Fig.1)
- Additions (a wish list) to specifications as a result of the CERN 99 test beam run:
  - base line restoration
  - cross-talk
- Results of calibration from CERN 99 test beam and P2" integration work in Oct-Nov 99 at Fermilab

## Calibration with injection boards and with the cathode strip

- **With injection boards**
  - $Q_{thr}$ calibration with use of known $C_{cal}$=1.6 pF ±5% and pulse generator (Fig.2a,b)
  - temporarily, only for AD96 boards with input cables
  - alternative solution (for 16 ch plug-in boards) is a test pulse from ALCT to the chip (new, under design, yet to be tested)

- **Thru the cathode strip**
  - unknown $C_{cal}$ though it can be estimated from comparizon with injection boards (Fig.3a,b)
  - reveals the features of P2" anode layout
  - available in P2' and P2" CSC, baseline
  - works for 16 ch plug-in cards
  - provided for each plane, allows to estimate cross-talk between planes
  - allows to measure a propagation time and relative chip delays

## Propagation time with the test pulse thru the P2” cathode strip

- **Direct measurement of delay with scope (N.Bondar)**
  - resistors disconnected
  - strip length of 332.7 cm (V.Razmyslovich)
  - propagation time
    $18.8 \pm 0.5$ nsec for layer 1
    $18.2 \pm 0.5$ nsec for layer 2
  - average inverse speed
    5.56 nsec/m or 0.28 nsec/wire group

- **Propagation time from the data**
  - signal propagates from the wide side of P2”
  - AD96D boards used
  - mean of time distribution in each channel (Fig.4)
  - discontinuities due to different delays in different chips
  - the slopes agree qualitatively with direct measurement

## Conclusion

- **Test thru the cathode strip allows:**

  **- to measure $Q_{thr}$ if $C_{cal}$ is known**
  **- to measure relative chip delays**