First Anode Front-End Mass Production Test Results

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Outline

- Anode front-end boards first shipment.
- Preamplifier chips test.
- Delay chips test.

Anode Front - End Boards

- The first shipments to UF and UCLA FAST sites
  - sent out on Oct. 2 and received
  - 124 boards for each site
  - Qthr = 25 fC at Uset = 150 mV
  - noise 2 fC
  - resolution time 0.5 - 1.0 ns
  - propagation time 70 ns
  - slewing time 2.5 - 3.0 ns

Anode Front - End Boards

- **Monitoring delivery Web page**
  - **http://www-hep.phys.cmu.edu/cms/delivery/AFEB**
  - **where, when and how many**
  - **distributions of parameters**
  - **table of the key parameters for use in FAST site tests**
  - **more details available soon in database at CERN**
  - **FAST sites report to CERN database AFEB's ID and location on CSC, CSC type and number**

Preamplifier CMP16G chips test

- Conditions
  - total 25,000 chips, about 2,500 tested
  - two chips tested per time in clamp shell connectors on ASIC test stand
  - 150 mV threshold setting, Cdet=0 pF, Cinj=1 pF
  - pulsed by high precision generator
  - measure threshold Qthr, noise, slewing time
  - test rate about 300/day

Preamplifier CMP16G chips test

- **Selection**
  - online analysis only
  - reject chips with dead channels and large current draw > 120 mA/chip (~8%)
  - require max. noise < 0.8 fC and max. Qthr deviation from average < 4 fC
  - require max. slewing time < 3 ns
  - require max. deviation in propagation time < 2 ns
  - less than 1% failed criteria above

Delay D16G chips test

- Test on the stand
  - two chips tested per time on ASIC test stand
  - test rate 250 - 300 chips/day, about 1,600 from 25,000 tested
  - online rejection if bad delay control or failed any test bit (3%)
  - measure mean time vs delay code (0 – 15) for each channel
  - needs offline selection due to large spread of delay from chip to chip

Delay D16G chips test

- **Offline analysis of delay chips data**
  - straight line delay vs code fit for each channel
  - offset 23 ns (initial delay), slope 2.5 ns
  - about 60% passed criteria
- **The delay chips selection criteria**
  - Max(Max – Min) delay < 4 ns
  - Max. Abs.(Fit – Data) delay < 2 ns
  - Aver. Offset 23 +- 1 ns
  - Max.Abs(Max,Min – Aver) Offset < 1.5 ns
  - Aver. Slope 2.5 +- 0.3 ns
  - Max.Abs(Max,Min – Aver) Slope < 0.2 ns
  - Differential Slope 0 – 3.5 ns