Mass Production Testing of the Anode Front-End Electronics for the CMS Endcap Muon Cathode Strip Chambers

A. Golyash*, N. Bondar*, T. Ferguson**, L. Sergeev*, N. Terentiev**, I. Vorobiev**

*) Petersburg Nuclear Physics Institute, Gatchina, 188350, Russia
**) Carnegie Mellon University, Pittsburgh, PA 15213, USA
(e-mail: golyash@fnal.gov)

Abstract

Results are reported on the mass production testing of the anode front-end preamplifiers and boards (AFEB), and their associated controllable time delay ASICs for the CMS Endcap Muon Cathode Strip Chambers. A special set of test equipment, techniques and corresponding software were developed and used to provide the following steps in the test procedure: a) selection of the preamplifier/shaper/discriminator ASICs for the AFEBs, b) test of the functionality of the assembled AFEBs at the factory, c) an AFEB burn-in test, d) final certification tests of the AFEBs, followed by the loading of all test information into a production database, and e) certification test of the controllable delay ASICs. A total about 12,200 boards have been tested, with a yield of more than 95%. Similarly, we have tested a total of about 24,000 delay chips, with a yield of 88%.

I. INTRODUCTION

The Anode Front-End Electronics (AFEE) [1] is designed and produced for the Cathode Strip Chambers (CSC) [2] of the CMS Endcap Muon System [3]. Its main purpose is to provide with high efficiency precise muon timing information for the LHC bunch crossing number identification at the Level-1 trigger. The large number of channels (more than 150,000) of the CMS Endcap Muon Anode System and the long term operation time (at least 10 years) with limited maintenance access require very high reliability of the anode front-end electronics.

The goals of the mass production test of the anode front-end electronics are:

- assure the quality of the anode front-end electronics which includes reliability, channel and board uniformity, and good timing performance;
- measure and certify the basic parameters of the boards;
- produce complete documentation needed for installation checkout, commissioning and maintenance.

The main part of the AFEE is a 16-channel Anode Front-End Board (AFEB) AD16[1], carrying a 16-channel preamplifier/shaper/discriminator ASIC CMP16[2] chip and associated components. The second important part is a 16-channel time delay ASIC DEL16. This chip is located at the input of the Anode Local Charge Tracker (ALCT) – a logic module for finding muon tracks in the chamber [4]. This chip receives signals from the AFEB and prepares them for the ALCT by converting the LVDS signal standard to CMOS signal levels.
It provides the required input pulse width of ~ 40 ns and aligns the input pulse phase with an accuracy of ~ 2 ns. The design characteristics, performance and preproduction test results of the anode front-end electronics, including burn-in and radiation tests, were reported earlier [1, 5].

The mass production test data and results are stored in a production database [6] for detector calibration and simulation purposes, as well as for board traceability. The status of the test and the results were monitored during the entire period of the mass production test [7].

II. THE ANODE FRONT-END ELECTRONICS TEST STEPS

The first step of the test is the acceptance of the CMP16 ASICs for installation on the AD16 boards (during the microcircuit production the manufacturer tested only the quality of the wafers). The following tests are used to select good chips on the CMP16 ASICs test stand: a) measurement of the AFEB current consumption (100 mA ± 10%); b) functionality checking of all 16 channels; and c) measurement of critical dynamic parameters for each channel by varying the input charge. The ASIC's threshold, noise, and propagation time must be within a given range for each parameter. Failure of any test leads to rejection of the ASIC. The yield of good chips was 90% for the total number of tested chips of 25,000. The dominant failures were large current consumption, dead channels and significant deviations of threshold or propagation time in one channel.

The second test step was performed by the AFEB manufacturer after the board assembly with the installed CMP16 ASIC. In addition to the high quality requirements and

[1] AD16 stands for a 16-channel amplifier/discriminator board.

[2] CMP16 is an abbreviation for a 16-channel ASIC designed by a collaboration of Carnegie Mellon University and Petersburg Nuclear Physics Institute.

control of the fabrication process, the manufacturer used our test equipment and our technique to check the board functionality and assure the quality of the board assembly. This test includes only a threshold measurement. The rejected boards were visually examined to find and fix most of the board assembly mistakes.

Before the final test, the assembled boards went through a burn-in procedure. The goal of the burn-in test is to increase the board reliability by detecting most of the hidden defects. During the 72-hour long test at a temperature of 90°C, the boards were powered and pulsed by a generator. The burn-in time was selected as 1% of the equivalent AFEB reliability test duration. The estimation of the AFEB reliability was made earlier [1] by burning in 100 boards in an oven for 4000 hours at a temperature of 110°C (equivalent to about 7 years of real operation at 30°C). Every two weeks the board parameters were measured. During the test, no failures were observed and all parameters of these 100 boards were stable. In the mass production burn-in test of 12,200 boards, only 30 boards were found not operational. The only reason was bad solder contacts, which were easily fixed.

The final AFEB test and its results are given in Section IV. The same section also describes the DEL16 delay chip test.

III. TEST EQUIPMENT

Four specially automated test setups have been developed and used for the mass production test. Each setup has two types of CAMAC modules - a specially designed precise pulse generator and a LeCroy 3377 TDC (standard module set), as well as a specific adapter for each setup. Three adapters are used in the three stands for testing the CMP16 ASICs and AD16 boards at different production testing stages:

- 2CMP16A - adapter for testing two CMP16 ASICs in two commercial clamshell connectors;
- 2AD16A - adapter for two AD16 boards. It is used for the assembly test at the factory and for a quick test during repairs;
- 10AD16A - adapter for the final test and certification of ten AD16 boards at once.

Each adapter receives a test pulse with a precise amplitude from the pulse generator and simultaneously injects charge into each amplifier channel (equivalent injection capacitance is 1.6 pF). The adapter also emulates the necessary detector capacitance (180 pF).

Adapters 2CMP16A and 2AD16A are used in corresponding test stands equipped with one standard module set. The stand for the final test and certification of the AD16 has the 10AD16A adapter and five standard module sets. All three stands have the same general structure (Figure 1).

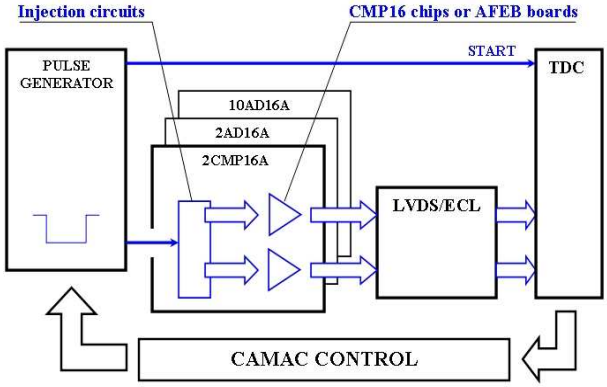

Figure 1: General structure of the CMP16 ASIC and AD16 board test stand.

The pulse generator produces a START signal for the TDC and a synchronized test pulse with a programmable precise amplitude and a rise time of 10 ns for the adapter. It also supplies power for the board and a programmable threshold voltage for the CMP16 discriminators. A 32-channel LVDS/ECL converter matches the CMP16 or AD16 LVDS standard outputs to the ECL standard of the TDC inputs. It is located in the pulse generator module. The LeCroy 3377 TDC (with a resolution of 0.5 ns) is used as the main DAQ module.

The fourth test stand is designed for testing the delay chips (Figure 2). This stand has one standard module set and its own specific 2DEL16A adapter with two commercial clamshell connectors to host the two DEL16 ASICs.

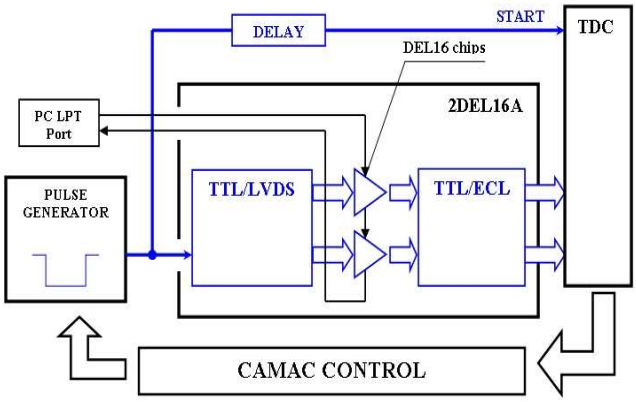

Figure 2: The DEL16 test stand structure.

The DEL16 test setup uses START pulses from the pulse generator to feed the 2DEL16A adapter and start the TDC. The 2DEL16A adapter converts the input NIM pulse to an LVDS signal and sends it to the DEL16 inputs. The adapter converts the DEL16 output pulses from TTL standard to ECL for matching the LeCroy TDC inputs. The delay chips are controlled by a PC through an LPT port (Figure 2).

Each stand is controlled with an Adaptec 2940 SCSI PCI Adapter and a Jorway 73A CAMAC Crate Controller by a PC using a device driver [9]. The data acquisition and on-line software uses Borland C++ code running in the NT Windows environment.

The sensitive analog electronics test equipment requires careful grounding. This was even more complicated because of the neighboring CAMAC electronics with the chip/board adapters. Therefore, every adapter had a carefully organized internal ground, and the ground connection between the adapter and CAMAC was separately optimized for each setup.

IV. MEASUREMENT METHODS AND RESULTS

A. AFEB final test and certification

The final AFEB test includes measurements of the following characteristics for each AFEB channel: threshold, noise, gain, discriminator offset, time resolution, propagation time, slewing time and internal test capacitance. The DAQ interface allows the operator to set all the conditions of the test: the minimum amplitude of the test signal, the amplitude increment, the number of steps, and the number of input pulses at each amplitude. The number of pulses recorded by the TDC for each value of the amplitude is used to obtain the threshold curve. The mean and RMS of the TDC time distribution for each amplitude of the input pulse give correspondingly the propagation time and the time resolution.

Each board is measured four times at different conditions, providing four sets of data: three threshold measurements and one timing measurement. The first two sets of threshold measurements have two different discriminator settings of 150 mV and 300 mV. They are taken with the test pulse going through the injection circuits of the adapter and the signal inputs of the board. The test pulse amplitude is varied around the ASIC thresholds. These data are used to get the corresponding thresholds and noise in terms of the input charge, as well as the preamplifier gain and the discriminator offset. In the third set, the discriminator setting is 150 mV but the test pulse feeds each CMP16 ASIC channel through its own internal capacitance, with nominal value of 0.25 pF. The technological variation of this capacitor may be up to 20% of its nominal value. The real value of each internal capacitor is calculated in the off-line analysis using the ratio of the threshold in the third set to the threshold obtained in the first set. The measurement of the internal capacitance is an important issue, because the use of this capacitance provides the only possible threshold calibration test for the board when it is installed on the chamber.

The timing parameters of the boards are measured in the fourth set of data taken at the same conditions as in the first threshold measurement. However, the amplitude of the test signal is varied through the full scale of the pulse generator. The results are the resolution and propagation time dependencies versus the input charge. The slewing time is defined as the difference between the maximum and minimum values of the propagation time observed in the region from approximately two to twenty times the threshold at a discriminator setting of 150 mV.

The on-line analysis of the data allows us to display and to check promptly the coarse values of the basic board parameters, such as threshold, noise and propagation time, against their allowed limits, providing the first level of board rejection. An example of the on-line display test for the threshold and noise is given in Figure 3. The value of the tested parameter for each channel is presented as a colored bar. If a parameter is out of limits, the corresponding bar becomes red, signalling the problem to the operator.

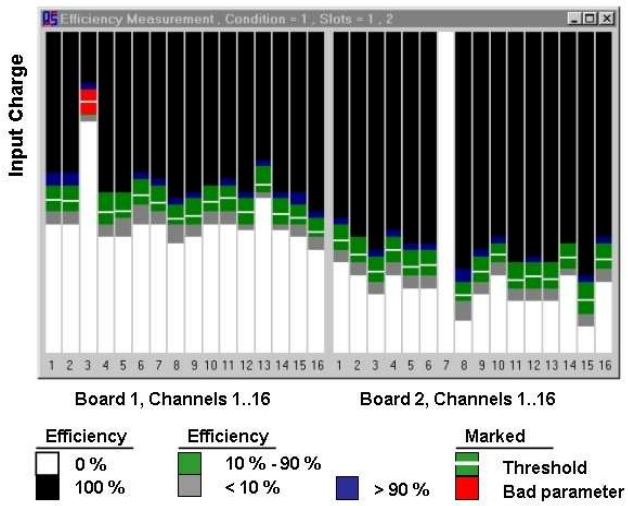

Figure 3: The AD16 board test stand display.
Channel 3 of board 1 has a large threshold deviation.
Channel 7 of board 2 is dead.

The data for the boards which pass the on-line criteria are analyzed off-line with use of ROOT [8], where the final values of all parameters for each board are calculated. For example, the threshold curve is fitted by a cumulative distribution function which includes a Gaussian error function with two free parameters - a mean as the threshold and a standard deviation as the noise. The results for each board are filtered through the set of certification cuts. The cuts impose limits on the average over the 16 channel values of the parameter and on the maximum deviation of the parameters from their averages to assure good uniformity of the parameters within a board. For the noise, time resolution and slewing time, instead of the maximum deviation, we use the maximum value of each parameter. As an example, the distributions of the threshold and noise averaged over the 16 channels of each certified board are presented in Figures 4 and 5, respectively, and the distribution of the maximum slewing time in Figure 6.

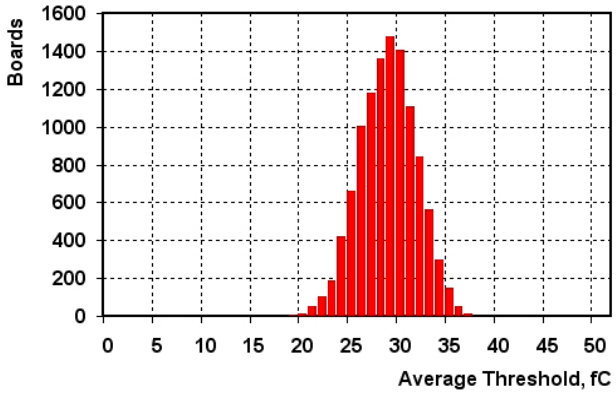

Figure 4: The average threshold for the AD16 boards.

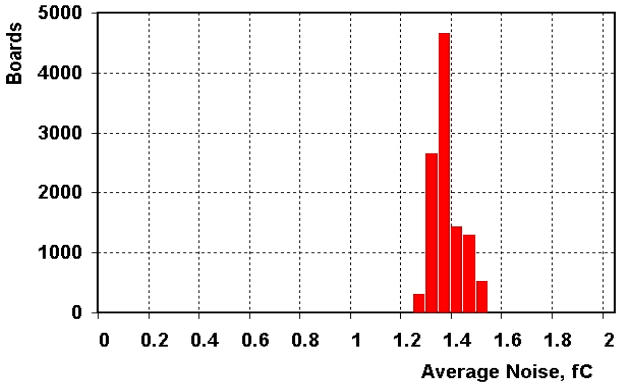

Figure 5: The average noise for the AD16 boards.

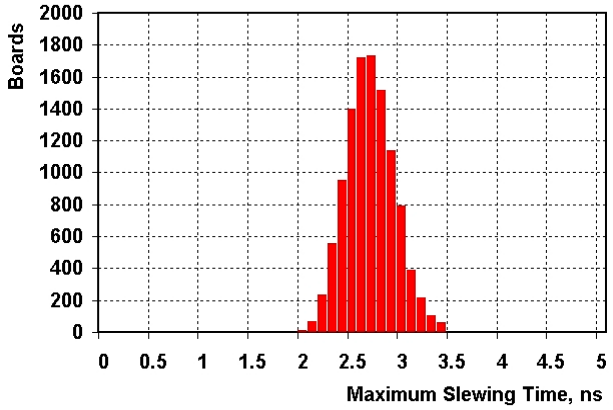

Figure 6: The maximum slewing time for the AD16 boards.

Table 1 presents a summary of the parameters for the certified AD16 boards. The threshold, noise and time parameters are from the first set of data with a discriminator threshold setting of 150 mV. The first column gives the mean value and standard deviation (RMS) of the distribution for each parameter averaged over all the channels of the board. Note that the average threshold is a controlled parameter and the spread of the average propagation time will be compensated by the controlled delay in the delay chips DEL16 on the ALCT. The results in the first column do not include any systematic errors which are of the order of 10-20% (conservative preliminary estimate). The actual average slewing time is higher by about 0.6 ns from the measured AFEB slewing time value due to the pulse generator's intrinsic slewing time contribution. The uniformity of the channels within each board is characterized in the second column as the standard deviation (RMS) of the channel residual, defined as the difference between the channel parameter and its value averaged over the 16 channels of each board.

Table 1: Summary of the measured parameters for the certified AD16 boards.

Parameter	Average	Uniformity
Threshold (fC)	29.2 ± 2.9	0.9
Noise (fC) at Cdet = 180 pF	1.4 ± 0.06	0.05
Transfer function (gain, mV/fC)	6.9 ± 0.3	0.07
Discriminator offset (mV)	50 ± 19	6
CMP16 chip internal capacitance (pF)	0.24 ± 0.02	0.01
Propagation time (ns) at Qin = 100 fC	66.5 ± 1.5	0.3
Slewing time (ns) at Qin = 50-550 fC	2.4 ± 0.2	0.2

The stability of the AFEB test stand is monitored through data taken each day using the same set of ten boards assigned to each of the 10 slots of the 10AD16A adapter. The largest changes in the slewing time for the monitoring boards are shown in Figure 7. They do not exceed ± 0.4 ns.

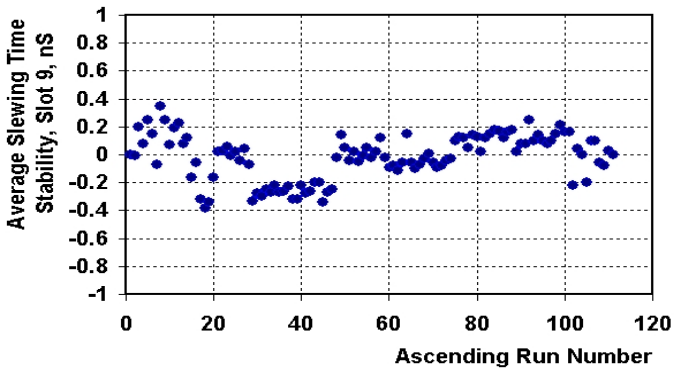

Figure 7: The largest average slewing time change for monitoring boards with adapter 10AD16A.

During the test, the weekly yield of good boards was about 90%. Most of the failed boards were quickly repaired, making the final yield above 95%. All raw data, test conditions, calibration constants and results of the off-line analysis are stored in the production database. This is an Oracle application [6], installed on the central CERN Oracle database. The data will be used for documentation purposes, by the CMS CSC Final Assembly and System Testing sites in the USA, Russia

and China and during CMS operation. Data are accessible through Web connections from standard Web browsers (using the Oracle9i Application Server and stored PL/SQL procedures).

B. DEL16 delay chip certification

The delay chip test stand measures the propagation time of the chips. The propagation time is controlled by the delay code, which varies from 0 to 15 with an average delay step of 2 ns. The test also checks the test level feature of the chips [1]. The selection of good delay chips is made on-line using the test stand. Chips having dead channels or faulty control of the delay or test level are rejected without any further on-line analysis. Parameters of the functional chips are checked against the list of acceptance criteria. The most important are the delay uniformity across the 16 channels of the chip at each delay code and the linearity of the delay versus code dependence. The main problem with the delay chip test stand was a degradation of the contacts of the commercial clamshell connectors. The clamshell connectors were replaced regularly after approximately 3000 connections.

A total of about 24,000 delay chips were tested, with a yield of accepted chips of 88%. Due to the technological spread of the average delay step, the accepted chips were divided into 9 separate groups, each having a 2 ns wide bin in the distribution of the average chip delay at a delay code of 15, see Figure 8. Groups from 5 to 8 (78% of the accepted chips) were used for the ALCT board production. The average delay steps for these groups can be tuned later on the ALCT boards.

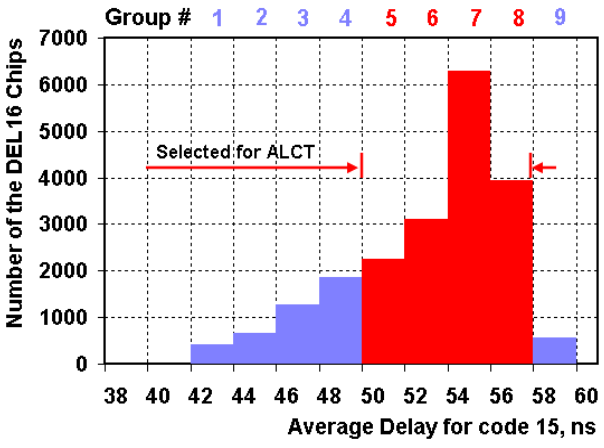

Figure 8: The distribution of the average delay showing the division by groups.

V. CONCLUSIONS

A specialized set of test equipment, techniques and corresponding software has been developed and successfully used for the mass production test of the anode front-end electronics for the CMS Endcap Muon Cathode Strip Chambers.

The anode front-end boards AD16 and delay chips DEL16 have been tested. The quantities of certified electronics are enough to equip all the chambers of the CMS Muon Endcap System. The performance expectations based on the preproduction experience have been confirmed in the mass production test. The data and results are stored in a central Oracle database at CERN for future use during the CMS experiment.

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VI. REFERENCES

1. N. Bondar, T. Ferguson, A. Golyash, V. Sedov and N. Terentiev "Anode Front-End Electronics for the Cathode Strip Chambers of the CMS Endcap Muon Detector", Proceedings of the 7-th Workshop on Electronics for LHC Experiments, Stockholm, Sweden, 10-14 September 2001, CERN-LHCC-2001-034.
2. D. Acosta et al., "Large CMS Cathode Strip Chambers: design and performance", Nucl. Instr. Meth., A 453:182-187, 2000.
3. CMS Technical Design Report - The Muon Project, CERN/LHCC 97-32 (1997).
4. J. Hauser et al., "Wire LCT Card", http://www-collider.physics.ucla.edu/cms/trigger/wirelct.html.
5. T. Ferguson, N. Terentiev, N. Bondar, A. Golyash and V. Sedov, "Results of Radiation Tests of the Anode Front-End Boards for the CMS Endcap Muon Cathode Strip Chambers", Proceedings of the 7-th Workshop on Electronics for LHC Experiments, Stockholm, Sweden, 10-14 September 2001, CERN-LHCC-2001-034.
6. R. Breedon, M. Case, V. Sytnik and I. Vorobiev, "Database for Construction and Tests of Endcap Muon Chambers", talk given by I. Vorobiev at the September 2001 CMS week at CERN, http://www-hep.phys.cmu.edu/cms/TALKS/cms_01_sep_ivorob.ps.
7. "CMS Endcap Muon Anode Front-End Electronics Project at CMU", http://www-hep.phys.cmu.edu/cms.
8. "ROOT: An Object-Oriented Data Analysis Framework", http://root.cern.ch.
9. J. Streets, D. Slimmer, "Windows NT®4 Device Driver and IEEE CAMAC Routines for the Jorway 411S SCSI CAMAC Driver and the Jorway 73A SCSI CAMAC Crate Controller", Fermilab preprint PN532, March 14 2001. We want to thank D. Slimmer of Fermilab for helping us with the driver installation.